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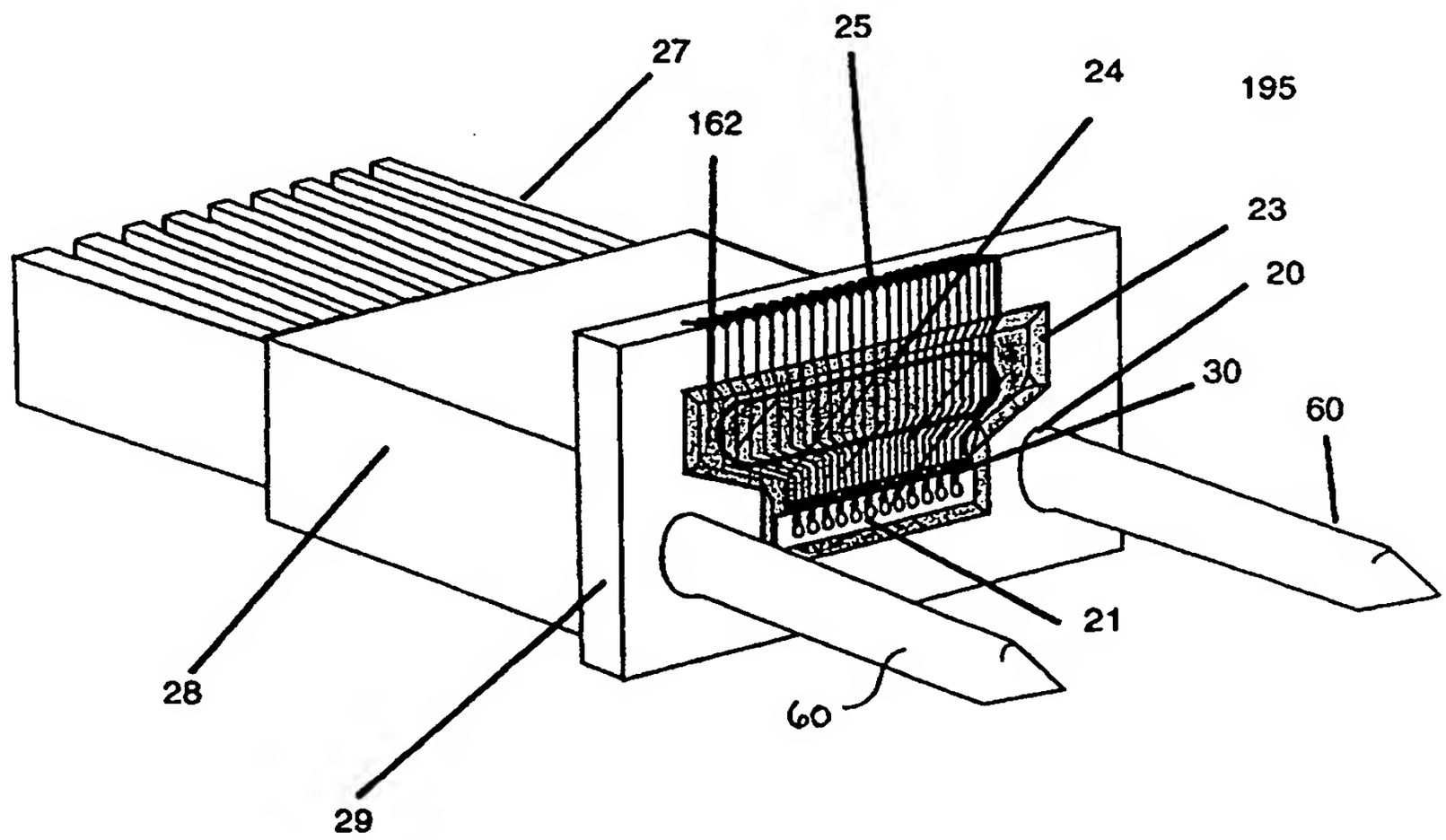

(57) Abstract

A substrate (29) for use in the manufacture of optoelectronic modules includes a coherent member having two parallel front and back surfaces, a trench (23) on the front surface and providing a locating mechanism for an optoelectronic device (21), and alignment apertures (20) in the coherent member adapted to receive alignment portions affixed to a component of the optoelectronic modules. The substrate serves as a platform for the optoelectronic device and as a cooperative guiding member for assembly of the optoelectronic modules.

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Optoelectronic Module and Method of Making same

Background of the invention

To date designs and methods of manufacturing photonics transmit/receive modules have relied on complicated techniques of aligning the light emitting and detecting elements, of encapsulating said elements, and of combining the carrier with a optical connector. This is especially true of arrays combining one or more light emitting or detecting devices in parallel. Attempts at handling Vertical Cavity Surface Emitting Lasers or VCSELs and their arrays, as well as photodetectors and their arrays for use in fiber Tx, Rx and Tx/Rx packages have often involved changing the optical axis of the chips--allowing them to interface with v-grooves in a silicon substrate such as in US Patent No. 5,337,391. Other groups have employed methods to change the optical axis that employ the use of angle polished fiber or flexible waveguide arrays such as Hewlett Packard's Parallel Optical Link Organization (POLO) [Hahn, K.H. PLOL "Parallel optical links for gigabyte data communications", in the Proceedings of the 45th electronic Components and Technology Conference Proceedings, pgs. 7-8]. Other designs have involved several complicated parts such as US Patent No. 5,337,398, or have involved the mounting of devices on an optical jumper block US Patent No. 5,719,978 or on the endface of a polished fiber array block such as in the Motorola Optobus [Schwartz, D.B., C.K.Y. Chun, B.M. Foley, D.H. Hartman, M. Lebby, H.C. Lee, C.L. Sheih, S.M. Kuo, S.G. Shook, and B. Webb, 1995, a low cost, high performance optical interconnect. In the Proceedings of the 45th Electronics Components and Technology Conference, pgs. 376-379. Piscataway, New Jersey : IEEE]. All of these references are hereby incorporated by reference herein. One prior attempt at monolithic integration using stacks of self aligned chips utilized ball lenses between the stacks to couple optical fibers to the optically active device as was seen in US Patent No. 5,259,054.

These earlier methods of handling optically active elements, especially surface emitting or receiving devices as arrays--as well as positioning of discrete components--has been very complex, expensive, and lacking in simplicity of design thus making the designs non usuable in the current manufacturing climate. The current invention relates to a new technique for creating a "face-plate" module for handling such active devices. The invention has wide application in making connection to existing and future parallel optical fiber array connectors in its ability to use modified existing ferrules and their alignment mechanisms and accurately align the optical elements of the carrier to the optical fibers.

This eliminates all need for expensive and hard to machine components, costly labor machining and complicated assembly techniques. The device is exceptionally useful for creating cost effective small form factor transceivers and parallel Tx/Rx modules. The invention allows a greater degree of monolithic integration than previously possible and eliminates many of the parts and steps previously required such as optical jumper blocks, polishing operations, etc. Such steps are very expensive to perform and time consuming thus adding to the price of the component member. The invention also will find application in chip to chip and board to board interconnects allowing easier cost effective packaging of the optical elements.

New and existing technologies in micromachining of silicon and other materials allow a greater degree of precision to be obtained in forming cavities and holes in substrates. For example the Bosch process has demonstrated through-wafer etching with excellent control of dimensions at etch rates making new mechanical structures possible. Newer deep dry etching technologies and wet anisotropic technologies—that have already been demonstrated in silicon wafers in conjunction with better encapsulants—make manufacture of these devices possible at this time. It is expected similar etching technologies will become available for other ceramic, glass, injection or transfer molded plastics, and other materials. In addition, parts of the design may find economic manufacture in the future using molding processes, laser machining, light/laser assisted chemical machining, etc.

The devices disclosed are various embodiments of a novel carrier for utilizing one or more optically active devices or elements (here meaning lasers such as VCSELs and VCSEL arrays, photo detectors and photodetector arrays, Light Emitting Diodes or LEDs, Super Luminescent LEDs or SLEDs, etc.) allowing them to be precisely positioned, electrically connected, encapsulated, optionally lensed, and heat sinked. The applications include chip to chip, board to board, and fiber optic and especially fiber optic array transmit, receive and transceiver modules. The approach disclosed can eliminate the need for polishing an assembly to form an optical surface, active alignment of the active optical elements to the carrier, and/or active alignment of the carrier to a connector assembly. Patterned metallizations and solders become incorporated in this design using techniques such as shadow masking, lift-off, selective CVD metal deposition, and can be combined with plating using electroless methods or any of the known electroplating techniques.

Summary of the Invention

The invention disclosed addresses the previously discussed problems inherent in the prior art by providing a simple, easily manufacturable, passively aligned method of coupling an optoelectronic device to a fiber or fiber array with most steps integrated at the wafer level. The passive and self correcting feature of the alignment method provides for an efficient and simple component to be added onto already existing components thus making its incorporation into the manufacturing process a desirable goal.

In fashioning the present invention, the preferred substrate material is a silicon wafer in which many substrate portions can be machined before being diced or cleaved into many components. Other equivalent material may be substituted only if suitable machining technologies are developed. Machining of silicon is a new art form in the manufacture of electronic components on a mass scale and it is precision work.

In a preferred embodiment of the invention, a substrate comprises part of the subassembly--with a precisely machined or formed trench in which the optoelectronic device is placed and aligned, with metallized bond pads and circuit traces to which the device can be electrically connected, with encapsulant filling the trench to encapsulate the device and provide a molded surface for later optical coupling, and with precisely machined or formed through holes or angled edges which serve as alignment guides for alignment fixtures such as pins to come through. The substrate is then placed onto alignment pins of a fiber optic connector housing and bonded to the housing of the connector while the pins hold the substrate in alignment. The pins may later be removed or left in place. The bonded fiber optic connector can be machined or formed to house a back side heat sink and the electrical leads for the optoelectronic device and possibly drivers mounted in the substrate.

In another embodiment, the trench that houses the optoelectronic device can be machined in the back side of the substrate, and a smaller window can be machined in the front of the substrate for the device to show through. In cases where the light to be transmitted or received is at a wavelength where the substrate is transparent, the front side window need not be machined.

In a further embodiment, alignment trenches or grooves are machined or formed into the front or back surface of the substrate so that a fitted cylindrical or spherical object can be inserted. This mechanism allows a new substrate with the same feature (alignment trench) to be aligned to the cylinder or sphere, thereby to also be aligned to the first substrate.

In yet another embodiment, the circuit traces for the optoelectronic device can extend into and through (perpendicular to the surface) the substrate instead of lying parallel to the front or back surface. This allows for simple front to back side electrical connection. The metallized via holes can also be cut in half, allowing electrical connection access to the surface perpendicular to the surface in which the device is mounted. This feature becomes important when it is desirable to affix a flexible circuit member to the subassembly along the edge of the substrate. This feature also allows direct bonding or secondary substrate mounting with a solder bump connection.

In a still further embodiment, the encapsulant that encapsulates the optoelectronic device can be shaped or altered to form lenses, gratings, mirrors, waveguides or other optical elements. This feature allows for beam shaping and/or the redirection of the light to another optoelectronic or waveguiding device. It should be noted that holes can be machined right through the wafer or substrate for insertion of optical fibers adapted to transmit from one side of the wafer or substrate to the other.

Objects of the Invention

A first object of the invention is to provide a simple means of aligning a single or arrayed surface emitting or receiving optoelectronic device to a single or arrayed fiber optic connector, and

It is another object of the invention to provide an encapsulated trench for the device that eliminates the need for polishing.

It is yet another object of the invention to provide an improved optoelectronic module, and

It is still another object of this invention to provide a innovative method for producing an improved optoelectronic module, and

It is yet another object of this invention to provide a superior alignment guide and component for optoelectronic components utilizing guide pins and or beveled surfaces, and

It is still another object to provide an improved alignment component for optoelectronic devices which is incorporated directly into the device, and

Yet another object of this invention is to provide a method of making optoelectronic components where a large amount of steps are done facilitating wafer level integration of the method, and

Still another object of this invention it to provide an optoelectronic componet which provides a passively aligned platform for an active device yet still utilizes existing coupling components thus enhancing saved costs, and

Further objects include the use of a one time passive alignment and insertion of a optoelectronic carrier and coupler component to an existing assembly and the provision of a superior assembly, and

Other objects of this invention include optimal connections of the component to other components such as heat sinks, IC circuits and the like, and

These and other objects will become apparent and will be demonstrated in the following drawings and text showing that the disclosed invention offers an easily manufacturable, passively aligned solution to a photonics packaging problem that has only been solved previously by complex or costly designs.

Brief Description of the Drawings

Figure 1 is a perspective cut-away view of the present invention showing a male connector piece of an optoelectronic subassembly for coupling to the arrayed device on a substrate, and

Figure 2 illustrates a machined or formed trench in a substrate for providing alignment of an optoelectronic device,and

Figures 3a through 3e illustrate various embodiments of the machined or formed trench in a substrate, and

Figures 4a through 4c illustrate various embodiments of machined or formed trenches in the back surface of a substrate for the optoelectronic device to be placed face-first within, and

Figures 5a through 5q illustrate variously shaped through holes which allow for alignment by pins or other cylindrical alignment mechanism, and

Figure 6 illustrates metallized circuit traces and bond pads on a substrate, and

Figure 7 illustrates the addition of a solder eutectic pad and trace on a substrate, and

Figures 8a, 8e and 8i illustrate various ways to achieve perpendicular circuit access on the edge of a substrate, with Figures 8b, 8c and 8d representing cross-sectional features of Fig. 8a, Figures 8f, 8g and 8h representing cross-sectional features of Fig. 8b and Figs. 8j, 8k and 8l representing cross-sectional features of Fig. 8i, as shown, and

Figure 9 illustrates the placement of the optoelectronic device in its alignment trench along with ball wire bonds to metallized pads on the surface of a substrate, and

Figure 10 illustrates the use of a flexible circuit as a means to access the electrical circuit on a substrate, and

Figures 11a through 11e show the methods for providing metallization and, hence, electrical connection, to the back of a substrate with the use of through holes, and

Figure 12a illustrates the injection of a known volume and subsequent curing of an encapsulant that comes flush to the surface of the trench that houses the optoelectronic device, and Figure 12b shows a top view of the substrate of Fig. 12a., and

Figure 13a illustrates a different embodiment of the substrate, where the optoelectronic device alignment trench is on the back side of the substrate, and where the device's active area shows through an open window on the front side and Figs 13b show a top view of the substrate of Fig. 13a.

Figures 13 c and 13d show the metallization and encapsulation for the substrate of Fig. 13a , and

Figures 14a and 14b illustrate two embodiments of the encapsulation—where the encapsulant can be precisely formed to shape optical elements, and

Figures 15a through 15c illustrate the method by which a heat sink is placed within an optical connector housing and how the substrate and device subassembly can be simply aligned to the same connector housing—allowing coupling to the connector housing's mating optical connector, and

Figures 16a through 16c illustrate the alignment and connection of a fiber optic array connector to a subassembly

Detailed Description

Figure 1 illustrates a mating part of an optical connector, where the other part of the connector (not shown) is an arrayed or single waveguide or fiber optic connector with fibers or waveguides embedded therein. The connector halves are to be mated by means of the alignment pins 60. The optoelectronic coupler subassembly 195 illustrated is partly comprised of a substrate 29 which has in it a machined or formed trench 23 in which an optoelectronic device 21 is placed—that optoelectronic device being any device which receives or emits light, and especially in, but not limited to, the direction perpendicular to the substrate's 29 front surface. The preferred embodiment of the invention is where the device 21 is a Vertical Cavity Surface Emitting Laser or VCSEL. The device 21 can have ball wire bonds 30 that affix to bond pads on or in the substrate. Electrically conductive traces, bond pads, and solder 24 are deposited onto the surface of the substrate to allow for simple electrical connection from a fanout circuit to the optoelectronic device via ball wire bonds and/ or "flip chip" bonding to the traces. The electrically conductive circuits may be metal or may be diffused conductors in the substrate. The bond pads or solder bumps 25 at the top or front of the pictured substrate 29 can be electrically connected to flex circuit, wire bonds, ball grid arrays, or any fitting electrical connector. The trench 23 is injected with an encapsulant 162 which encapsulates the device 21 and can provide a flush, optically flat surface for coupling to the device 21 preferably without the need for polishing. Polishing has been required in the past due to the large amount of machining needed on the surface of the elements. Polished surfaces were needed to insure good face-to-face contact between surfaces and to provide good and complete contact for bonding. The encapsulant can also provide focusing, reflecting, or waveguiding optical elements to redirect light within its confines. The encapsulant can be molded or chemically altered to produce this effect, or a separate optical element can be embedded within its confines. The holes 20 through the substrate 29 are precisely machined or formed to provide precise alignment of the substrate 29 and the device 21 to any alignment pin or tool pushed through the subassembly's holes. Such an alignment tool can be the housing of an optical connector 28 that can have precisely positioned pins 60 for mating to the other half of its connection. The optical connector housing 28 can be machined or formed to accept a heat sink 27 that butts against the back surface of the substrate 29 to conduct heat away from the optoelectronic device 21.

Figure 2 illustrates the substrate 29 with its machined trench 23 and via holes 20. The trench 23 and the via hole 20 can be machined or formed into the substrate 29 so that they are in precise alignment with one another either through a parallel forming or machining mechanism or through a photolithography step that defines both areas at once, or uses precise mask and mask alignment. Trench 23 has beveled sides 31all around to provide for both a guiding feature and to allow any encapsulant to form correctly.

Figure 3 illustrates the various embodiments of the trench formed in the substrate 29 with alignment holes 41. Figure 3a illustrates a rectangular trench 40 having beveled sides 43 that shows the configuration of the trench if the substrate would be <100> silicon (or formed by means of a mold) and wet anisotropic etching machined the trench. This embodiment 40 also illustrates a smaller trench footprint for later illustration. The trench 42 in Figure 3b illustrates another trench formed or machined in the same manner as 40, but allowing for two separate optoelectronic device chips to be placed on the substrate along the direction of the width of the substrate due to the configuration of trench 42 which is also formed with beveled sides. Double trenches 44 in Figure 3c are formed or machined in the same manner as 40, but allow for two separate optoelectronic device chips to be placed in a parallel fashion on the substrate along the direction of the height of the substrate. The rectangular trench 46 in Figure 3d illustrates the machining or forming of a trench in a different manner—if the substrate would be <100> silicon (or formed by means of a <100> silicon mold) and deep reactive ion etching or DRIE machined the trench (or formed by means of a mold), or if the substrate would be <110> silicon (or formed by means of a mold) and wet anisotropic etching machining the trench which would be a parallelogram. Such a trench does not have beveled sides as shown. The two trenches 48 in Figure 3e illustrates are formed or machined in the same manner as 46, but allow for two separate optoelectronic device chips to be placed on the substrate along the direction of the width of the substrate. Not pictured is the option of the embodiment of a trench formed or machined in the same manner as 46, but allowing for two separate optoelectronic device chips to be placed on the substrate along the direction of the height of the substrate.

The optoelectronic device can be placed within the trench with its active area facing out of or into or along the surface plane of the substrate.

Figure 4 illustrates the various embodiments of trenches formed or machined in the substrate for placement of the optoelectronic device into the back surface of the substrate, where the active area faces into the substrate and a window is cut out on the front surface for the active area to show through. Windows are not necessary for wavelengths for which the substrate is transparent to the optoelectronic device. Trench 50 in Figure 4a

illustrates the use of wet anisotropic etching to machine the resultant front trench if the substrate would be <100> silicon (or formed by means of a <100> silicon mold) and the use of DRIE (or formed by means of the same mold) to form the back trench that aligns and houses the optoelectronic device. The result forms a lip 53 which acts as a stop to maintain an optoelectronic device in place and parallel to the disposition of the substrate 29. Trench 52 in Figure 4b illustrates the use of wet anisotropic etching to machine the resultant front and back trench if the substrate would be <100> silicon (or formed by means of a <100> silicon mold). The result is a beveled front trench 55 and a beveled rear trench 56 which form a lip as shown to provide a guide and stop to hold a component in place. Trench 54 in Figure 4c illustrates the use of DRIE in the back and front of the substrate (or formed using a mold for the substrate) to provide both trenches, the front trench having a inner surface 58 and the rear trench having a back surface 57 which provide an alignment and stop lip to secure a component in place. . Not shown is bonding the active device to the back side without a machining a trench for the device.

Figure 5 illustrates the various embodiments of the via holes machined or formed into the substrate 29 to provide for alignment to pins or alignment tools. A cut-away side view of a circular hole embodiment is pictured in Figure 5b with a top cross-sectional view provided in Figure 5a. This hole 62 is formed or machined via DRIE or laser drilling. The hole 62 is viewed face-on in Figure 5c with a pin 60 aligned within its edges. A cut-away side view of a diamond shaped hole embodiment 70 is pictured in Figure 5e with a top cross-sectional view provided in Figure 5d. The hole 70 is viewed face-on in Figure 5f. with a pin 60 aligned with four points of contact. The hole can be formed or can be machined via DRIE or laser drilling or using a wet anisotropic etch if the substrate material is <100> silicon and the angle of each of the hole's edges is 45° off the major flat angle. The square, straight-walled hole can be machined 45° rotated from what is pictured in 70 if the substrate is <110> silicon. A cut-away side view of a square shaped hole embodiment 78 is pictured in Figure 5h with a top cross-sectional view provided in Figure 5g. The hole 78 is viewed face-on in Figure 5i with a pin 60 aligned with four points of contact. The hole 78 can be formed or can be machined using a wet anisotropic etch. The hole 78 can be formed by entirely etching through the front side 74 of the wafer 29, entirely etching through the back side 76 of the wafer 29, or any combination of depths of either. A front cut-away side view of a square shaped hole embodiment 84 with beveled edges 85 in the front is pictured in Figure 5k and a back cut-away side view of a square shaped hole embodiment is pictured in Figure 5l, with a top cross-sectional view provided in Figure 5j showing the straight and beveled sides 85. One side of the hole 84 can be formed or can be machined using a wet anisotropic etch, while the other

can be formed or can be machined using DRIE or laser drilling. As illustrated in Figure 5n, a diamond shaped hole 70 can be cut to provide two points of contact 90 for pin 60 alignment as in the face-on view Figure 5m. As illustrated in Figure 5p, a square hole may be cut to provide three points of contact 92 for pin 60 alignment as shown in the face-on view Figure 5o. The multiple points of contact provide alignment and centering functions and, when mated back together, form four points of contact with a circular guide pin 60. As illustrated in Figure 5r, a circular hole may be cut to provide an arc of contact 94 for pin 60 alignment as shown in Figure 5q. Such an arc contact provides for a press fit of the pin 60 within the hole 62 on substrate 29.

Figure 6 illustrates an electrically conductive circuit 99 deposited onto or selectively diffused in the substrate 29 with its trench 23 and holes 20 . This circuit can provide bond pads 104 for ball wire bonds to the optoelectronic device and / or its drivers. The circuit fans out at 102 to provide easier access to the top bond pads 100. The circuit can include ground plane circuits between signal carrying circuits to provide less crosstalk between signals.

Figure 7 illustrates an electrically conductive solder pad 106 to allow for flip chip or direct bonding of the optoelectronic device and / or drivers to the substrate 29 with its holes 20 and trench 23. Patterned solders may be made to reflow to provide for alignment of the device with its bottom pads 104within the trench, or the trench walls used for the alignment.

Figure 8 illustrates various embodiments of the substrate providing for perpendicular and backside access to the circuits on or embedded in the front surface of the substrate 29 with its holes 20 and trench 23. In the circuits illustrated in Figure 8a., the edge conductors 110 are formed by anisotropic etching of <100> silicon or forming of some other material into the v-shaped trough 114 and depositing an electrical conductor on or diffusing a conductive layer into the surface. The substrate can then be cut to form two pieces as in Figure 8c., one of which becomes the chip shown in side cross-sectional view in Figure 8d with a sloped trough for receiving the array circuit. The edge connection 110 provides perpendicular access to the optoelectronic device's circuits. In the circuits illustrated in Figure 8e., the edge conductors 120 are formed by anisotropic etching of <110> silicon or DRIE or laser drilling of the substrate material or forming of some other material into the rectangular trough shape 122 and depositing an electrical conductor on or diffusing a conductive layer into the surface. The substrate can then be cut to form two pieces as is shown in Figure 8g., one of which becomes the chip as is

shown in side cross-sectional view in Figure 8h as a notched trough. The edge connection 120 provides perpendicular access to the optoelectronic device's circuits. In the circuits illustrated in Figure 8i., the edge metallizations 128 are formed by DRIE through the substrate material or forming of some other material into the shape 130 and depositing an electrical conductor on into the surface. The substrate is then cut to form two pieces as is shown in Figure 8k., one of which becomes the chip as is shown in side cross-sectional view in Figure 8l with its concave troughs for termination of the array circuit. The edge connection 128 provides perpendicular and backside access to the optoelectronic device's circuits.

Figure 9 illustrates the alignment and bonding of the optoelectronic device 21 into the alignment trench 23 of substrate 29. The shape of the trench, with its beveled sides, receives the device and aligns it at the same time, eliminating the need for further alignment. Ball wire bonds 30 affix the electrical connections on the front face of the device 21 to the bond pads in or on the substrate's surface.

Figure 10 illustrates the use of "flex" circuitry 150 connected to the edge circuit of the array to carry the electrical signals away from the substrate in a protective flexible conductor. The flex circuitry may be connected to the top edge circuit by any of the means heretofore described.

Figure 11 illustrates the use of via holes 155 to carry the electrical connections for the optoelectronic device to the back surface of the substrate 29 with its rectangular trench 40. Figure 11a. illustrates a cut-away side view, while Figure 11b. illustrates a cross-sectional side view. Various embodiments of the via holes with conductive layers are shown in Figures 11c-e. The embodiment of a straight hole 156 shown in Figure 11c. can be formed or can be machined by DRIE or laser drilling. The embodiment shown in Figure 11d. with its hourglass shaped hole 157 can be formed or can be machined by a combination of wet anisotropic etches into <100> silicon, one on the back surface and one on the front surface. The embodiment shown in Figure 11e.with its tapered hole 158 can be formed or be machined by wet anisotropic etch on one surface of a <100> silicon substrate. It should be noted that such deep holes could be made to house optical fibers perpendicular to the surface and the such holes could be made in an array for an opposing chip which would be used to form an independent fiber to fiber or fiber to device connection system.

Figure 12 illustrates the injection of a known precise quantity of encapsulant 162 to fill flush to the surface of the alignment trench 23. In Figure 12a., a cut-away side view of the substrate with circuit traces, solder, optoelectronic device, and encapsulant 162 is shown. The side cross-sectional view Figure 12b. illustrates the flat surface achieved by molding the encapsulant 162 flush to the surface of the substrate and curing it.

Figure 13 illustrates the method by which an optoelectronic device is fitted into the substrate 29 through the back surface trench as defined in 50, Figure 4a. The device 21 is fitted face-first into the back surface trench of 50 as in the top cross-sectional view Figure 13b. In Figure 13c., the back surface face-on view illustrates the conductive circuit traces and solder bond pads 24 for the device 21. In Figure 13d., the back surface face-on view illustrates the device 21 in place with its back facing out and its active area facing into the substrate. The lip 163 formed by the intersection of bevel 164 and straight side 165 holds device 21 in place in an aligned position.

Figure 14 illustrates embodiments of the molded encapsulant face to include, but not to limited to, optical elements like lenses and mirrors on a substrate 29. In Figure 14a., a lens 180, made of a rounded protrusion, spreads the light L coming out of the optoelectronic device 21 if 21 is a light emitting device, or 180 focuses the light L coming into the device 21 if 21 is a light receiving device. In Figure 14b., the device 186 is a light emitting device like a VCSEL, LED, or SLED, while the device 188 is a light receiving device like a PIN diode. A portion of the light transmitted from 186 reflects off of angular surface 182 into the active area 188, where it is detected. This configuration is useful for monitoring the power of 186. The angle of surface 182 can be calculated to provide for the correct amount of reflected light to impinge upon 188.

Figure 15 illustrates the fashioning of a optical connector housing 28 that has the same spacing and alignment as a mating connector with fibers or waveguides embedded in it. The optical connector housing 28 has alignment pins 60. It also has a feature such as slot 91that accepts a protrusion 92 on heat sink 27 into its body so that the optoelectronic device on the substrate 29 can thermally conduct through it. In Figure 15a., the connector housing 28 and the heat sink 27 are displayed separately. In Figure 15b., the heat sink and the housing have been assembled, and the optoelectronic coupler subassembly 195 is displayed separately. In Figure 15c., all the parts have been assembled. The subassembly 195 and the heat sink 27 would be affixed to the connector housing 28, but the pins 60 could be removed once the assembly 195 is bonded in place. The device is ready for connection via solder bumps 25 to an array, a circuit, drivers or the like.

Figure 16 illustrates, in Figures 16a, 16b and 16c the sequence of coupling of a fiber optic array connector 210 to the optoelectronic subassembly 205. The guide pins 60 used to align substrate 29 and component 28 have been removed as the two pieces were bonded. The fiber optic array connector 210 with its flex cord 211 has pins 160 which in turn are inserted into holes 20 of substrate 29 which previously received pins 60 for alignment purposes prior to bonding. Once 210 is inserted into holes 20 the device can be considered complete or it is further bonded together.

The invention herein allows for a large degree of wafer integration. It allows for the use of etching to provide for passive alignment of components within an assembly of components. A large plus to this invention is the utilization of existing components, such as those shown in Figs 15 and 16 as 28 and 210 respectively, in the subassembly. This negates the need for expensive manufacture of all new components to achieve this positive passive alignment while at the same time providing a superior platform for the technology. The invention allows for direct bonding of the device to the carrier or other component and for solder or patterned metallizations in the recesses. This allows for flip-chip bonding of pads on the active device to the carrier.

It also allows for possible ground plane metals extending between the traces to help prevent crosstalk in the final module. It also allows for connection to flex (metal conductors in/on a flexible medium) at a distance where there is no interference from the other connector or functions on the face.

The ability to accurately construct the trenches also allows for disposition of a known amount of transparent (can be non-transparent if other optical paths are chosen) encapsulant can be injected to form optical surface. It also allows for the insertion of a filter or other optical elements. This can incorporate coatings to change the reflectivity and transmission such as bandwidth, etc. The use of encapsulant protects against damage due to abrasion, water, and dust to the wire bonds. It is possible to emboss or otherwise shape the encapsulant to form a singular or array of small lenses to optimally couple the light in and out of the system. These can deflect the light to photodiodes to monitor the output of the light. Transparent slides can be inserted into the encapsulant to alter the light transmission qualities thereof.

The silicon wafers can be etched using wet or dry processes. The apertures can be metallized to pass signals from one side of the carrier to the other side. The use of CVD metal deposition and physical vapor deposition at a tilted or variable incident angle is also contemplated. Holes can be etched though the wafers or substrates using isotropic or anisotropic etching giving perpendicular access allowing subsequent

metallization of the trenches. The trenches can be filled with solder for connection to another substrate or board and can have pass through connections as described herein from both the edge perpendicular and the opposite side. I. e, the holes can be etched so as to pass electrical connections up to the top edge of the substrate as well as to the opposite side. The etching provides for passive alignment features both in the trench and the holes. A heat sink can be attached to the component with the active portion extending away from the heat generating device which enhances the operation of the sink.

The use of the guide pins and alignment system allows the component to serve as a one time alignment guide to fiber array ferrules which utilizes the mechanics of the fiber array for subsequent matings. The system also allows for board to board free space optical connection. Components having integrated ICs can be connected up as well.

An important consideration is that many of the steps in providing the components are integrated at the wafer level which allows for huge cost savings to be made. This allows also for greater thickness in face plates and requiring only minor changes to be made to the housings which connect and aligns the two ferrules.

Where the operation of devices is 1200 to 1600 nm. the carrier (substrate) is transparent the devices may be mounted facing the carrier in a etched recess. If the carrier is not transparent the cut-out section may be etched so as to be in communication with the trench. In such a case a non-transparent encapsulant may be utilized.

Having shown and described the invention in its many incarnations it will be obvious to those of ordinary skill in the art that many changes and modifications can be made without departing from the scope of the appended claims

1. A substrate for use in the manufacture of optoelectronic modules, said substrate comprising

a coherent member having two parallel front and back surfaces,

a trench on said front surface and providing a locating mechanism for a optoelectronic device,

alignment apertures in said coherent member adapted to receive alignment portions affixed to a component of said optoelectronic module,

whereby said substrate serves as a platform for said optoelectronic device and as a cooperative guiding member for assembly of said optoelectronic modules.

2. A substrate as in claim 1 wherein said substrate is made of silicon.

3. A substrate as in claim 1 wherein said trench has beveled or perpendicular sides which serve to guide and locate the optoelectronic device within said trench in a predetermined position.

4. A substrate as in claim 1 wherein said apertures comprise a pair of holes in said substrate, said holes being located in said substrate on each side of the area of said substrate in which said trench is located.

5. A substrate as in claim 1 wherein said trench is T-shaped.

6. A substrate as in claim 5 wherein there is a non-trench portion extending partially up the stem of the T.

7. A substrate as in claim 1 wherein said trench comprises two trenches extending parallel to one another.

8. A substrate as in claim 1 and including a cut-out area cut into said back surface and in communication with said trench area.

9. A substrate as in claim 8 wherein said trench and said cut-out area form a lip where they intersect, said lip adapted to form a seat for locating said optoelectronic device.

10. A substrate as in claim 8 wherein said trench has beveled or perpendicular sides.

11. A substrate as in claim 8 wherein said front trench is formed by wet anisotropic etching and said cut-out area is formed by DRIE.

12. A substrate as in claim 8 wherein said front trench and back cut-out area is formed by deep reactive etching.

13. A substrate as in claim 1 wherein said substrate is constructed of transparent material and the optoelectronic device wavelengths pass therethrough.

14. A substrate as in claim 1 wherein said trench is formed by means of a <100> silicon and wet anisotropic etching or by use of a mold.

15. A substrate as in claim 1 wherein said trench is formed of <100> silicon and DRIE.

16. A substrate as in claim 1 wherein said trench is formed of <110> silicon and wet anisotropic etching.

17. A substrate as in claim 1 wherein said alignment apertures are square holes adapted to linearly engage pins along points of contact.

18 A substrate as in claim 1 wherein said alignment apertures are square holes with corresponding beveled portions on said front and back surfaces of said substrate to provide a series of four contact points to a round guide pin or locating spheres.

19 A substrate as in claim 1 and including at least one hole extending from said trench to the back surface of said substrate for accommodating electrical connections.

20. A substrate as in claim 19 wherein said hole is circular.

21. A substrate as in claim 19 wherein said hole is hourglass shaped in cross section.

22. A substrate as in claim 19 wherein said hole is tapered in cross section.

23. A component for assembly into a optoelectronic module, said component comprising

a substrate having a front and rear surface,

alignment apertures in said substrate and adapted to accommodate guide pins for aligning and positioning said component relative to other components in said optoelectronic module,

at least one trench means on the front surface of said substrate,

an optoelectronic device located in said trench and adapted to cooperate with other components of said optoelectronic module,

whereby said component may be assembled in an aligned manner with said other module components by inserting guide pins of another component into said apertures.

24. A component as in claim 23 wherein said substrate is made of either <100> or <110> silicon.

25. A component as in claim 23 wherein said trench has beveled sides for locating said optoelectronic device in a preselected position.

26. A component as in claim 23 wherein said trench is formed by wet anisotropic etching.

27. A component as in claim 23 wherein said trench is formed by DRIE machining.

28. A component as in claim 23 wherein said optoelectronic device is a Vertical Cavity Surface Emitting Laser (VCSEL) or VCSEL array.

29. A component as in claim 23 wherein said optoelectronic device is a photo-detector or photo-detector array.

30. A component as in claim 23 wherein said optoelectronic device has ball wire bonds and said substrate has bond pads in said trench, said ball wire bonds affixed to said bond pads.

31. A component as in claim 23 wherein said optoelectronic device is affixed by solder pads on the device and/or solder pads on the trench by means such as flip-chip bonding.

32. A component as in claim 23 wherein said substrate has edge surface thereon, an array of electrically conductive circuits extending from said device and connected to said edge surface so as to be available to connect with other components that attach to said module.

33. A component as in claim 32 wherein said array is fan-shaped and said circuits terminate in solder bumps on said substrate edge surface.

34. A component as in claim 32 wherein said edge has a series of sloped troughs into which said circuits terminate.

35. A component as in claim 32 wherein said edge has a series of notched rectangular troughs into which said circuits terminate.

36. A component as in claim 32 wherein said edge has a series of concave troughs into which said circuits terminate.

37. A component as in claim 23 wherein said substrate is transparent to allow for passage of wavelengths of said optoelectronic device to pass therethrough.

38. A component as in claim 23 and including a cut-out area in the back side of said substrate, said cut out area in open communication with said trench and providing a direct optical path for optical signals from said optoelectronic device to other components in said module.

39. A component as in claim 38 wherein said cut-out area and said trench intersect to form a lip which acts as a seat for said optoelectronic device which is seated by pushing into said cut-out area.

40. A component as in claim 23 and including at least one hold between said back surface of said substrate and the trench to allow for electrical connections to other components of said module.

41. A component as in claim 40 wherein said hole is hourglass-shaped in cross section.

42. A component as in clam 40 wherein said hole is tapered in cross section.

43. A component as in claim 23 and including a cut-out area in the back surface of said substrate, said substrate and trench being in open communication with said device being located in said cutout area, a precise quantity of encapsulant filling said cut-out area and trench to encapsulate said device.

44. A component as in claim 23 wherein said trench is filled with a precise quantity of transparent encapsulant thereby encapsulating said optoelectronic device.

45. A component as in claim 44 wherein said encapsulant includes at least comprising an optical configuration in said encapsulant and said configuration is embossed or shaped to adjust the divergence or re-direct the light.

46. A component as in claim 45 wherein said optical configuration comprises a filter.

47. A component as in claim 45 wherein said optical configuration comprises a polarizer.

48. A component as in claim 45 wherein said optical configuration comprises a lens.

49. A component as in claim 48 wherein said lens is made of a rounded protrusion on said encapsulant.

50. A component as in claim 23 wherein said optoelectronic device is a light emitting device like a VCSEL, SLED or LED.

51. A component as in claim 23 wherein said optoelectronic device is a light receiving device like a PIN diode.

52. A method of providing for a large degree of silicon wafer integration from a wafer sheet of silicon, said method comprising

etching a plurality of alignment trenches in said wafers,

etching a corresponding number of guide apertures in said wafers in the general vicinity and in precise relationship to said alignment trenches,

severing sections of said wafer into individual substrates each containing at least one alignment trench and at least one guide aperture.

53. A method as in claim 52 wherein said method of machining is deep ion reactive etching.

54. A method as in claim 52 wherein said method of machining is wet anisotropic etching.

55. A method as in claim 52 wherein said trench is etched with beveled sides.

56. A method as in claim 52 wherein said step includes etching two parallel trenches.

57. A method as in claim 52 wherein the wafer is <100> or <110> silicon.

58. A method as in claim 52 and including the step of

providing metallization on portions of said wafer corresponding to said substrates to thereby provide electrical connection for the completed components.

59. A method as in claim 58 wherein said metallization is provided by either CVD metal deposition, by physical vapor deposition or by wet chemical processes.

60. A method as in claim 59 which includes the steps of providing holes in said wafer between substrates to provide surfaces for metal deposition which become circuit connection troughs once said substrates are severed from said wafer.

61. A method as in claim 52 and including the step of

etching a cut-out portion on said wafers directly opposite and in communication with said alignment trenches so as to provide optical passage for optoelectronic signals.

62. A method as in claim 52 and including the step of

locating and affixing optoelectronic devices in the trenches in such a fashion as to provide for electrical and optical connectivity with other components in an optoelectronic module assembly.

63. A method as in claim 62 and including the further step of

encapsulating said optoelectronic devices with a transparent encapsulant to provide protection therefore against dust, abrasion and water.

59. A method as in claim 57 and including the further step of

etching electrical connector holes in said wafer areas for allowing front to back connection and/or front to edge connection between an optoelectronic device in said trench with other components in an optoelectronic module.

60. An optoelectronic subassembly with several components including at least one component consisting of a hear sink, an IC circuit and a fiber optical array connector, said subassembly used in the field of photonics transmit/receive modules and comprising

a substrate having a trench thereon,

guides holes in said substrate cooperating with guide features on said other components,

an optoelectronic device located in said substrate trench and adapted to operatively cooperative with said other components.

61. An optoelectronic subassembly as in claim 60 wherein said optoelectronic device is a Vertical Cavity Surface Emitting Laser.

2

Figure 1

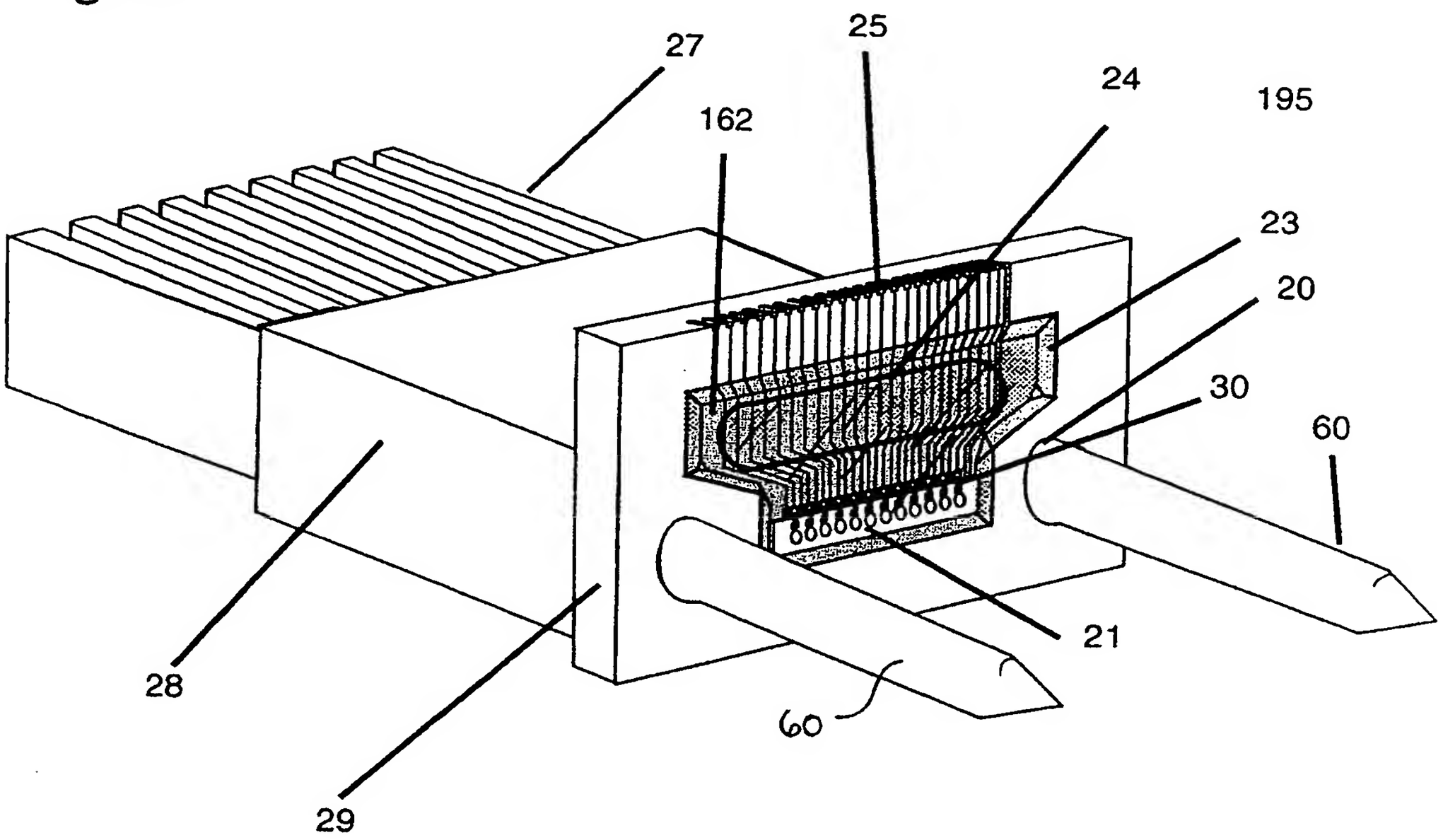


Figure 2

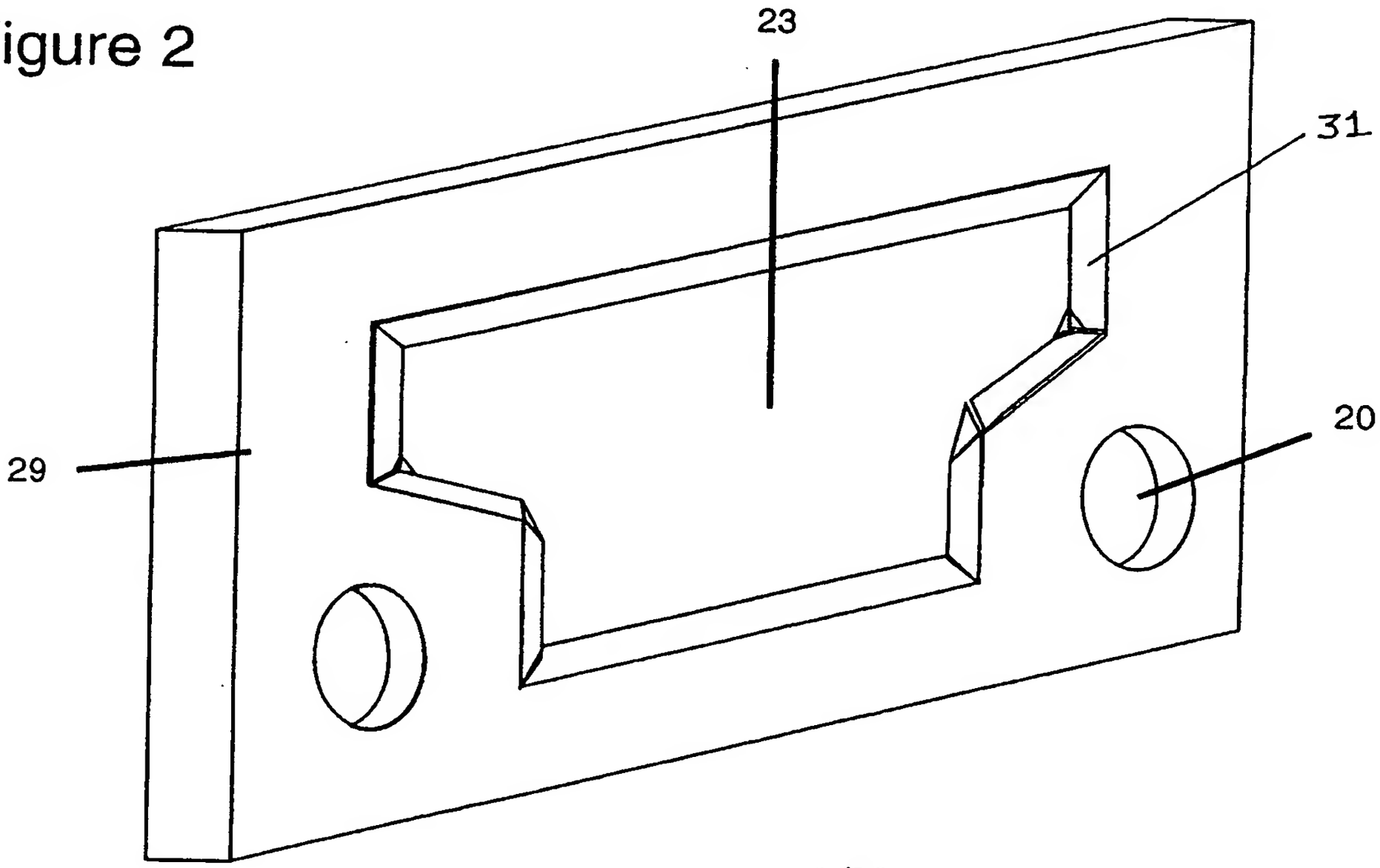
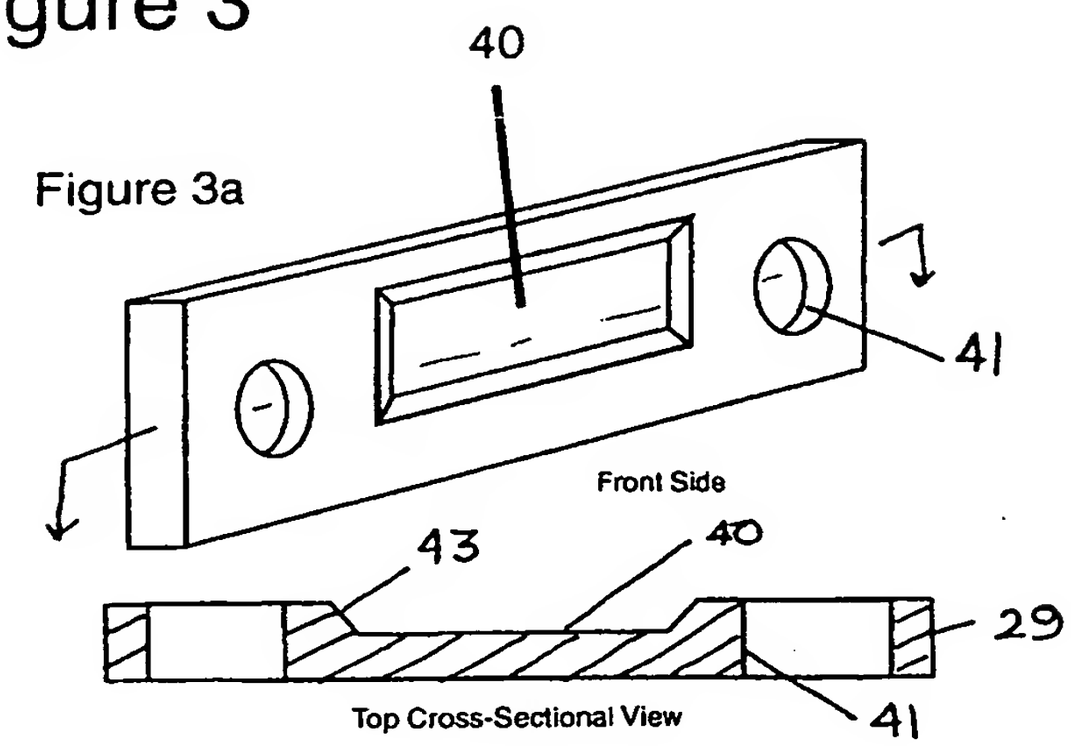


Figure 3

Figure 3a



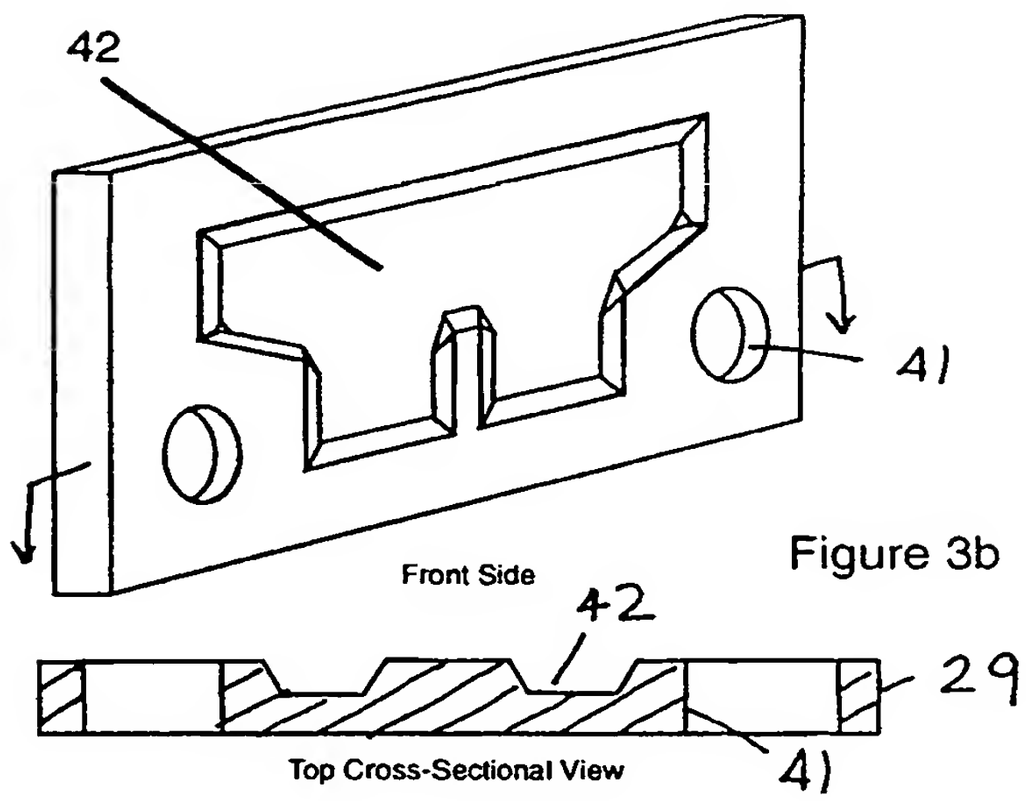
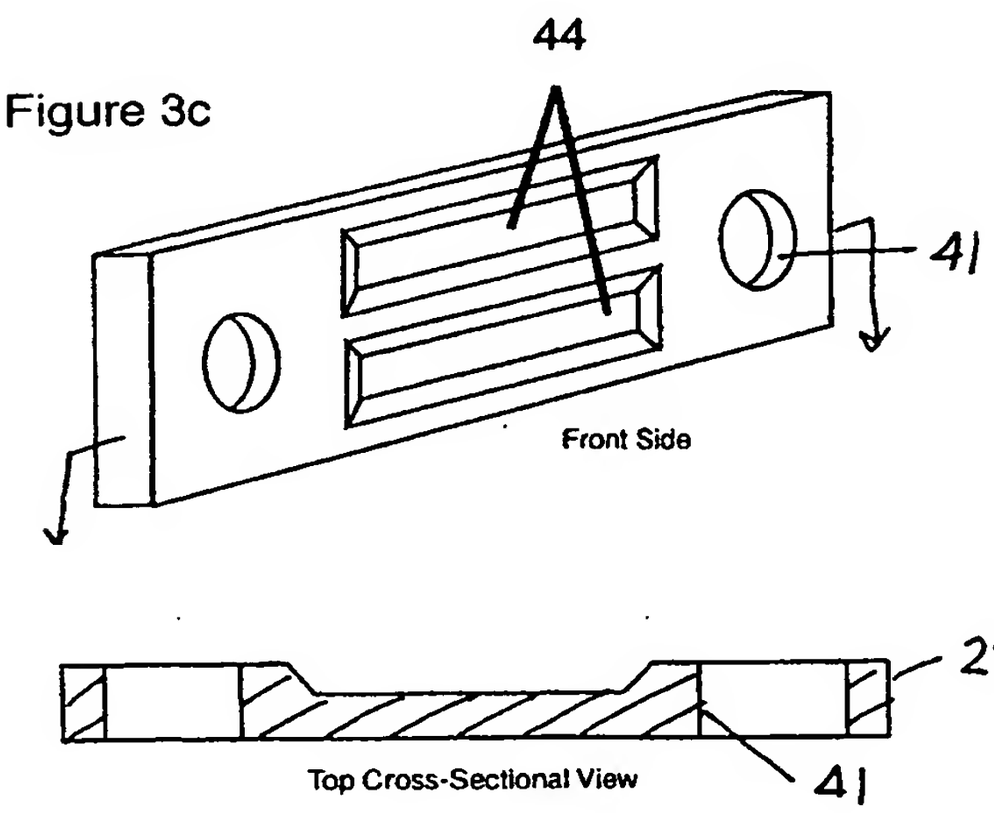


Figure 3b

Figure 3c



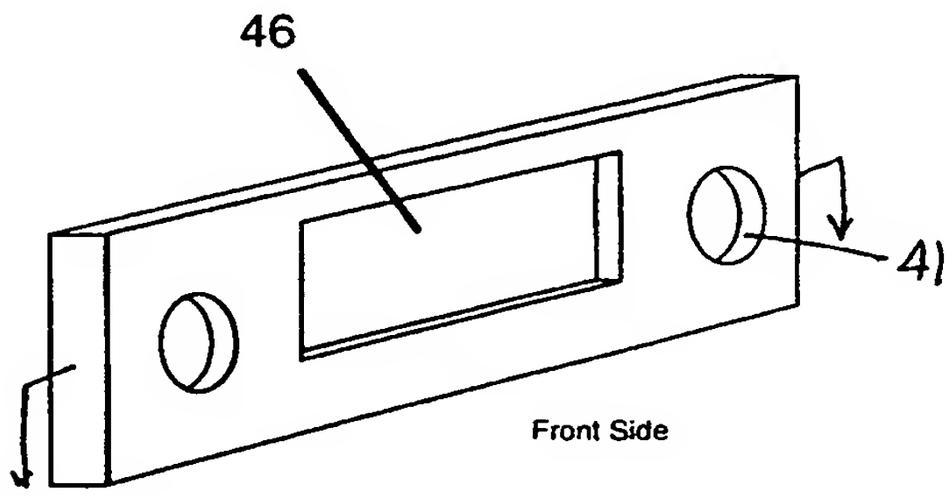


Figure 3d

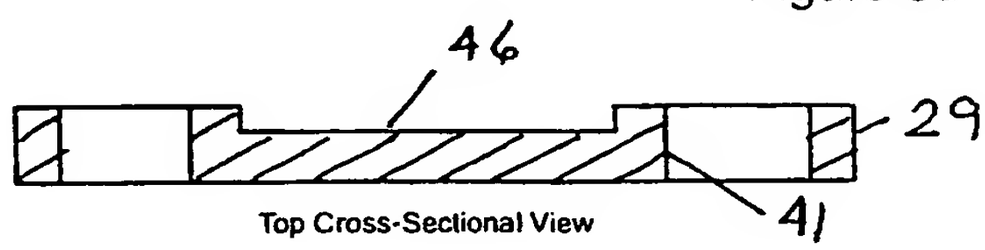
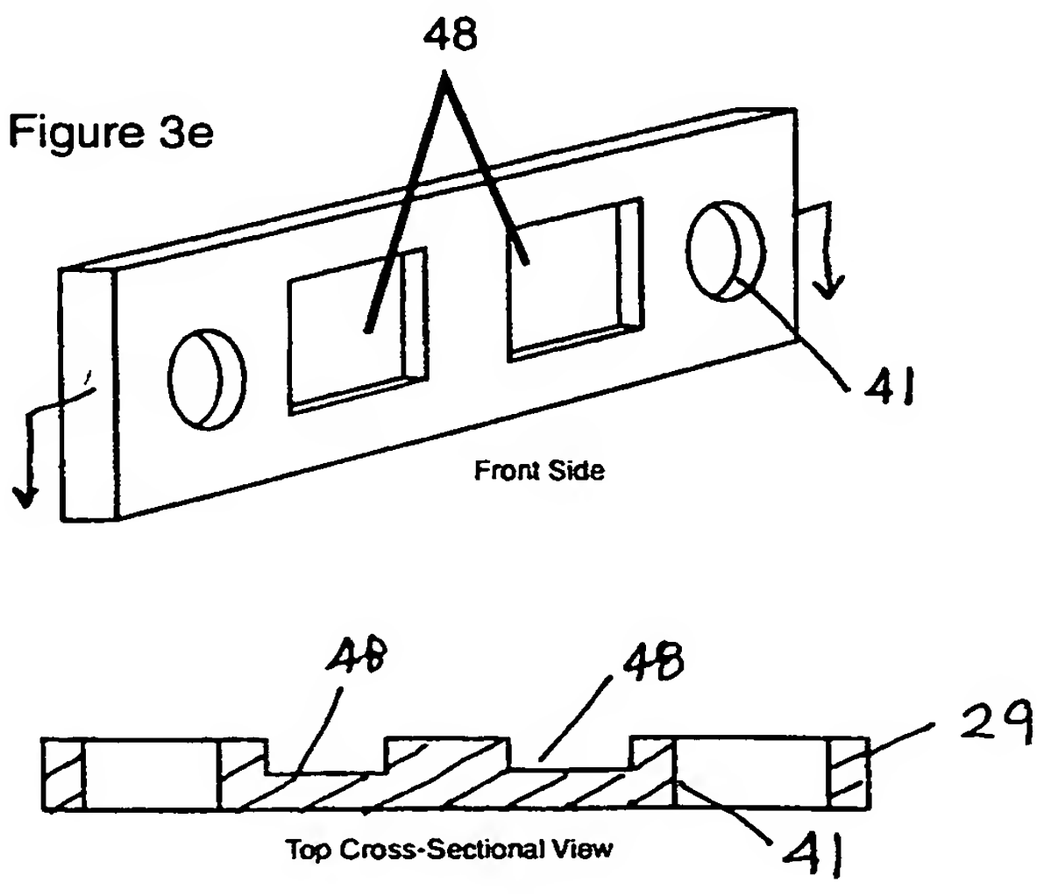


Figure 3e



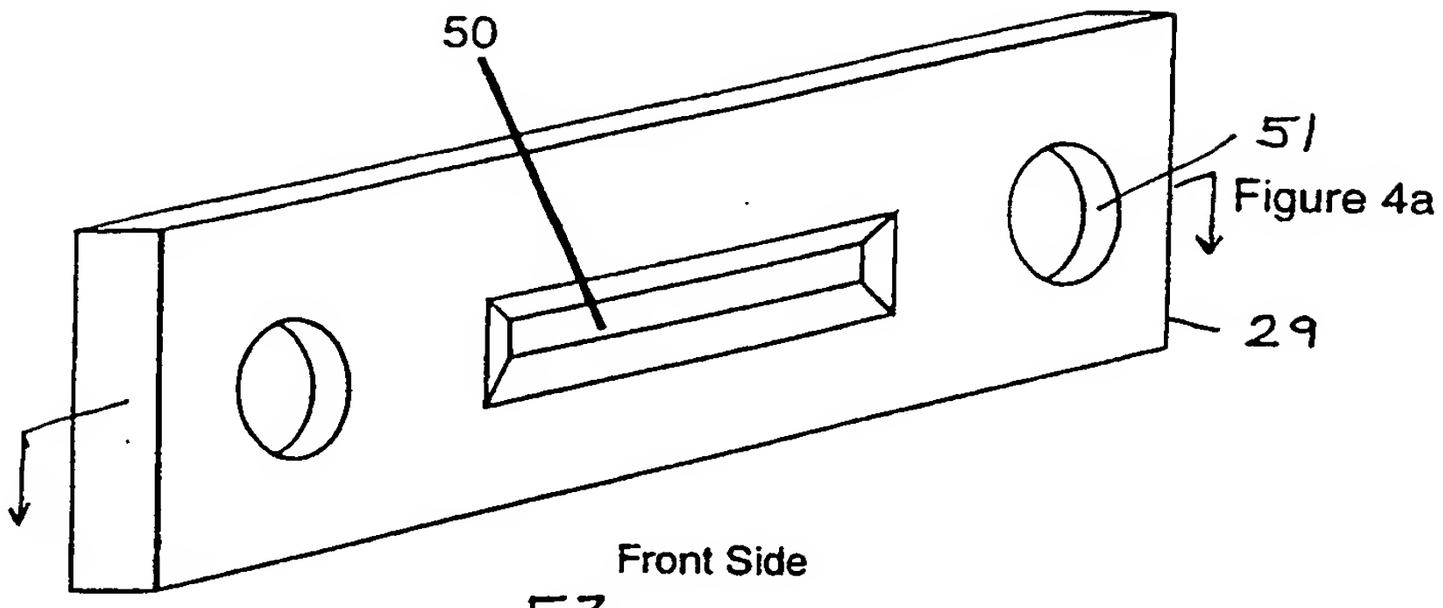


Figure 4

Figure 4b

Figure 4c

Figure 5

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Figure 6

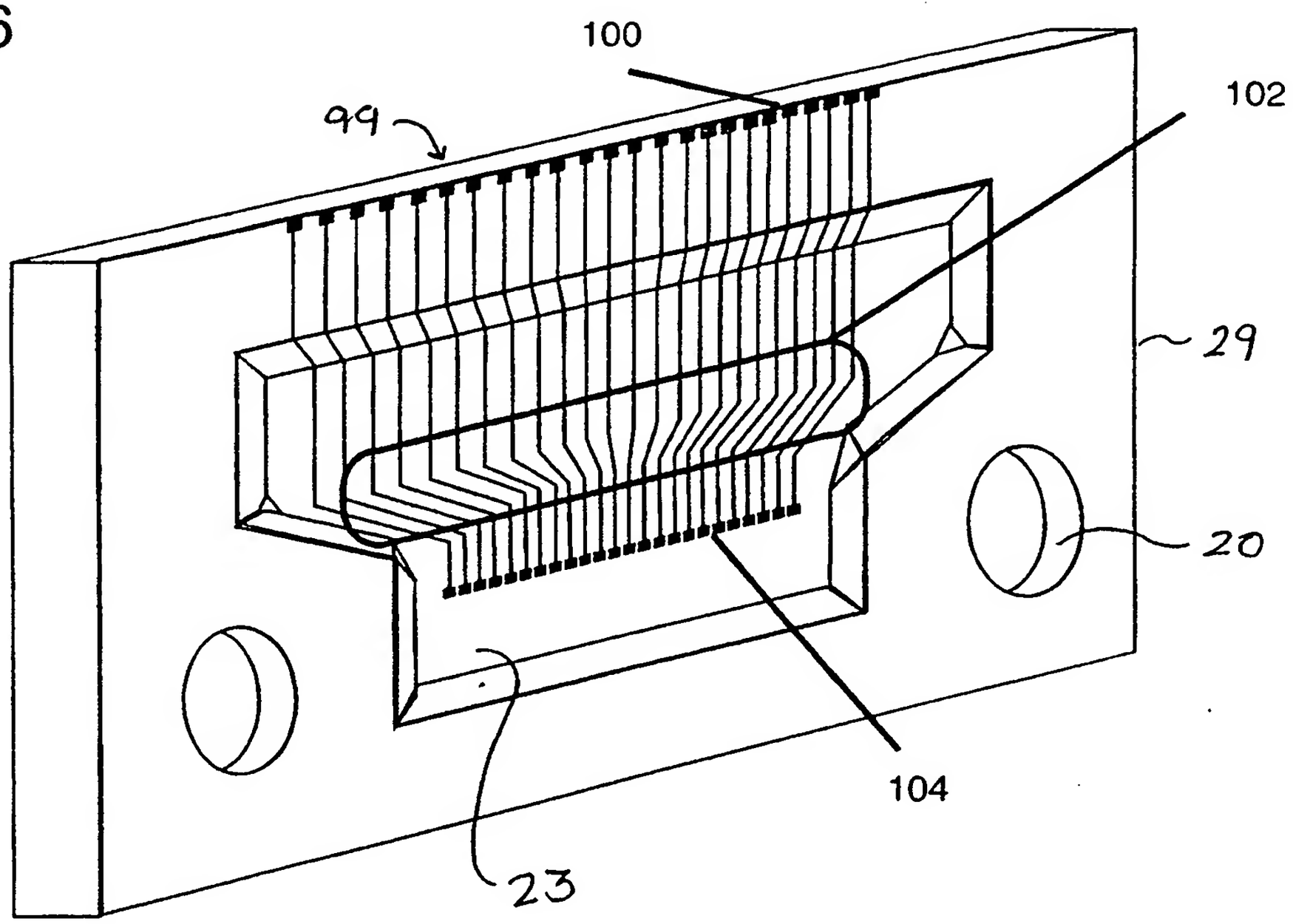

Figure 7

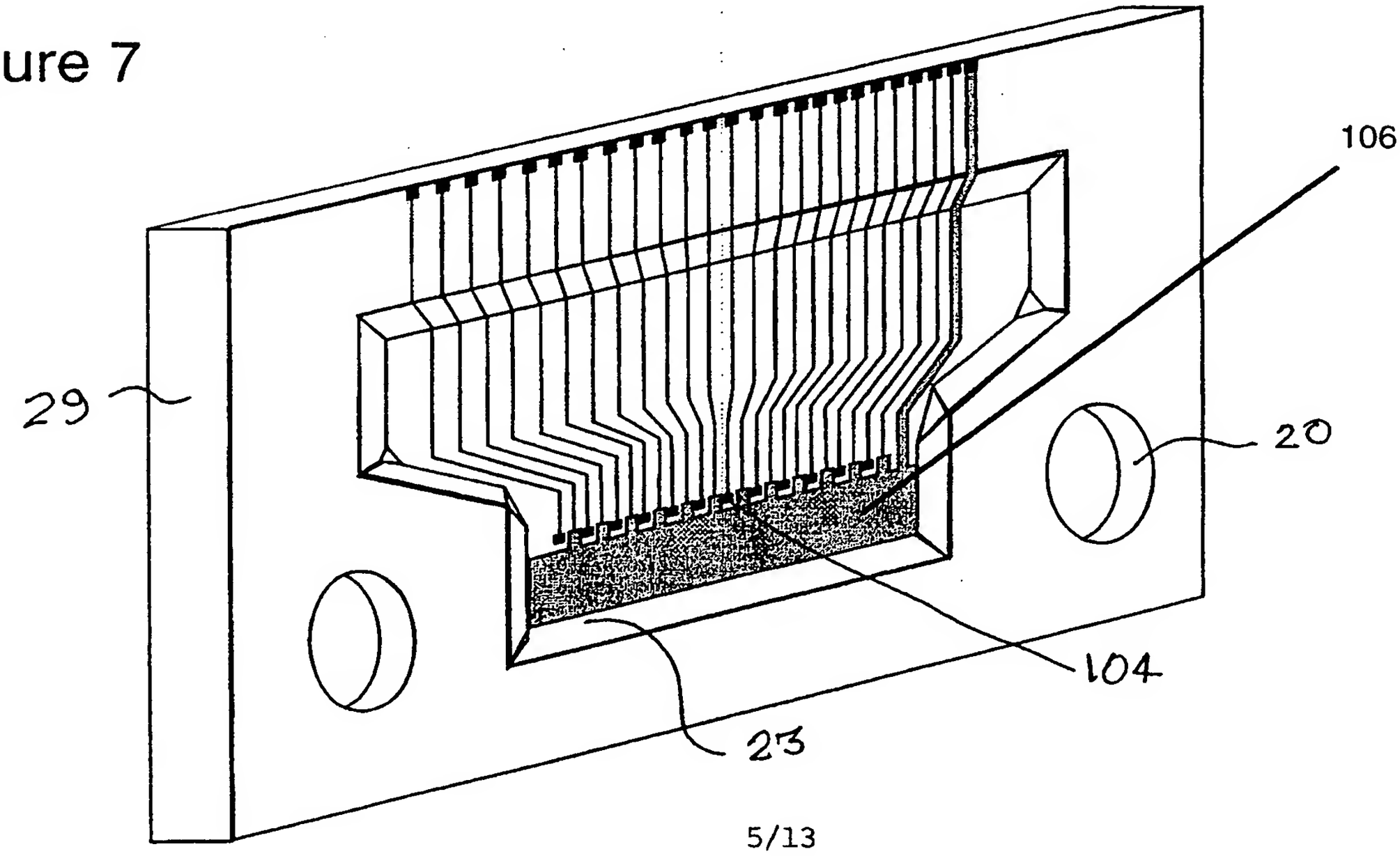

Figure 8

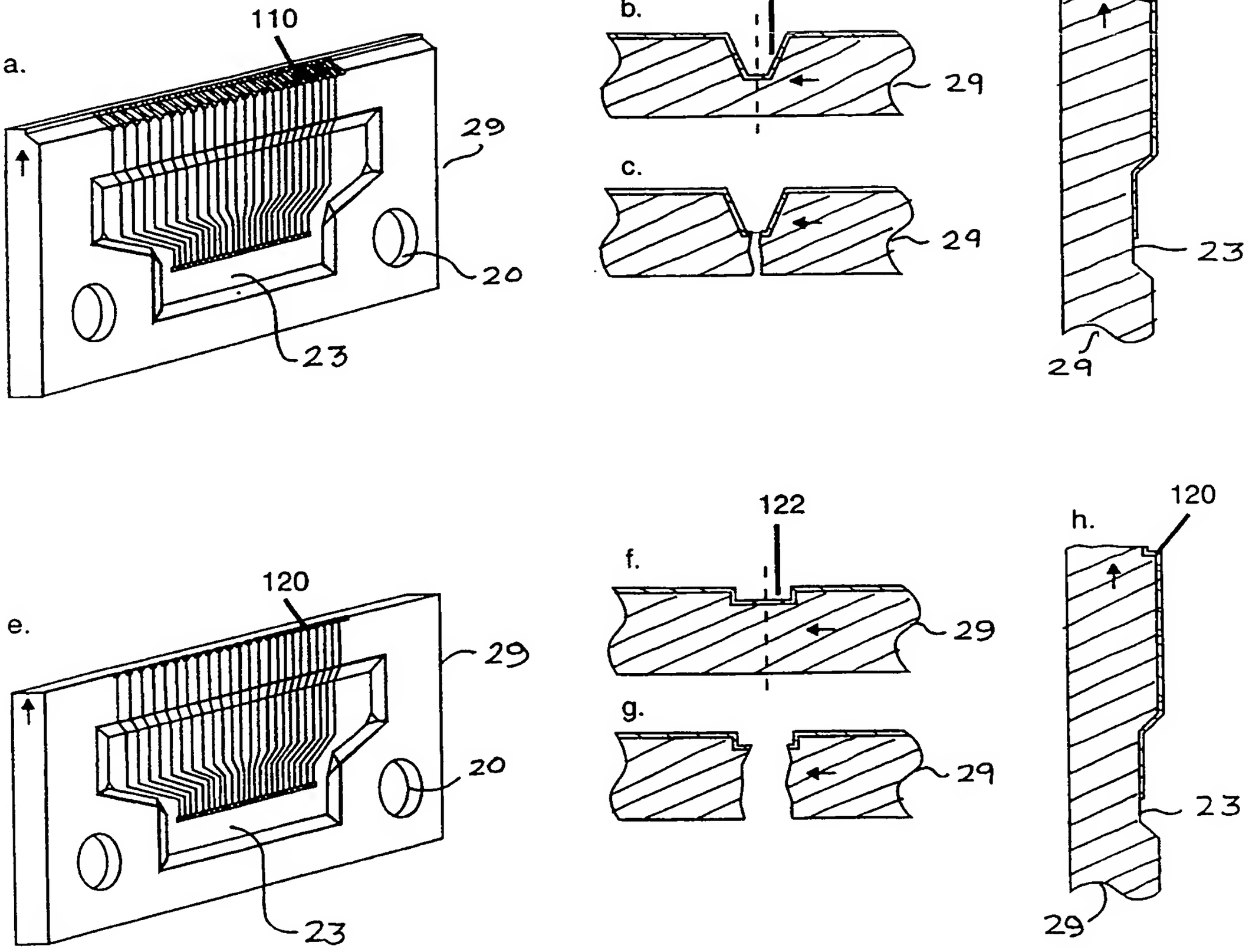
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Figure 9

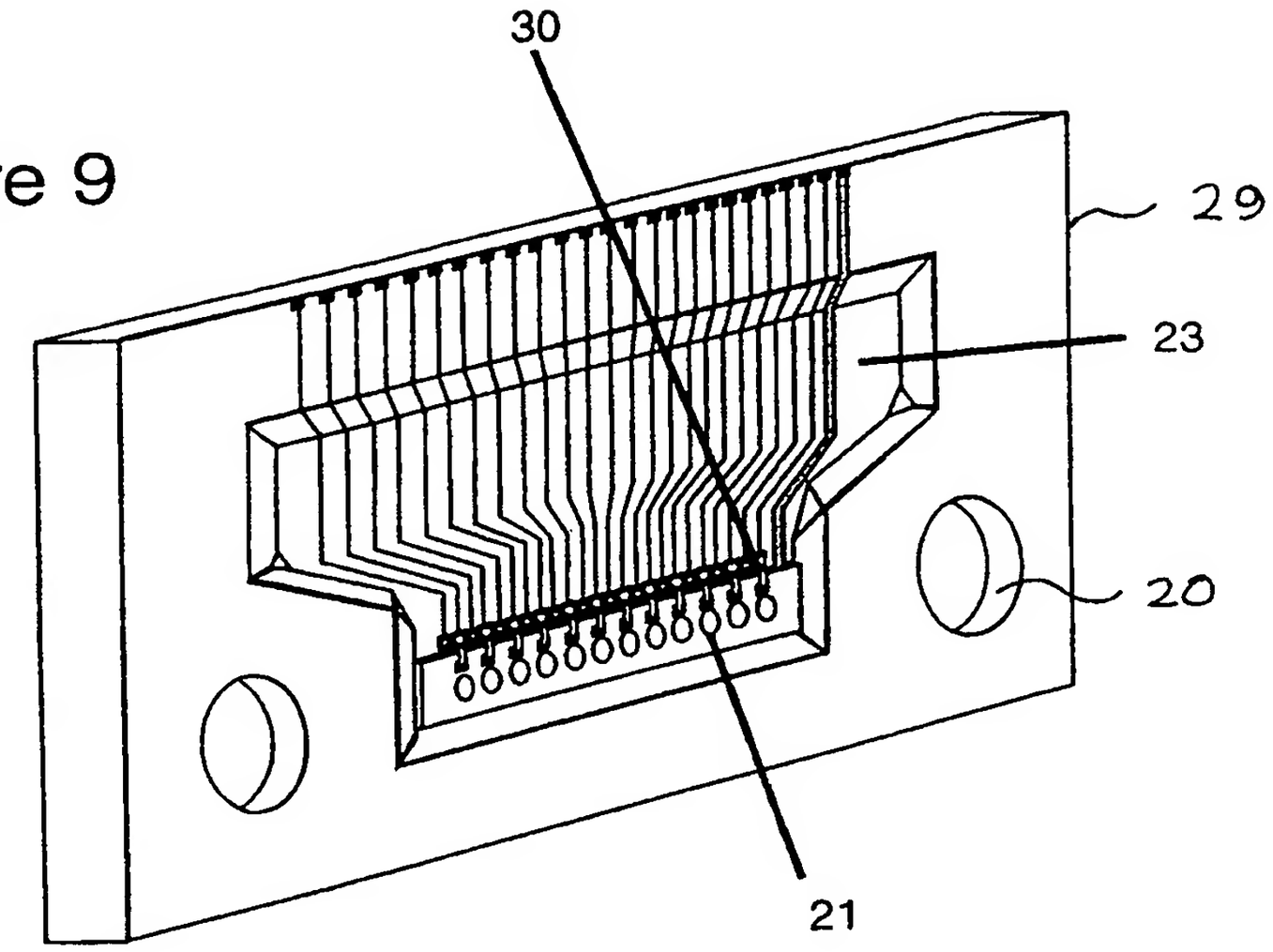
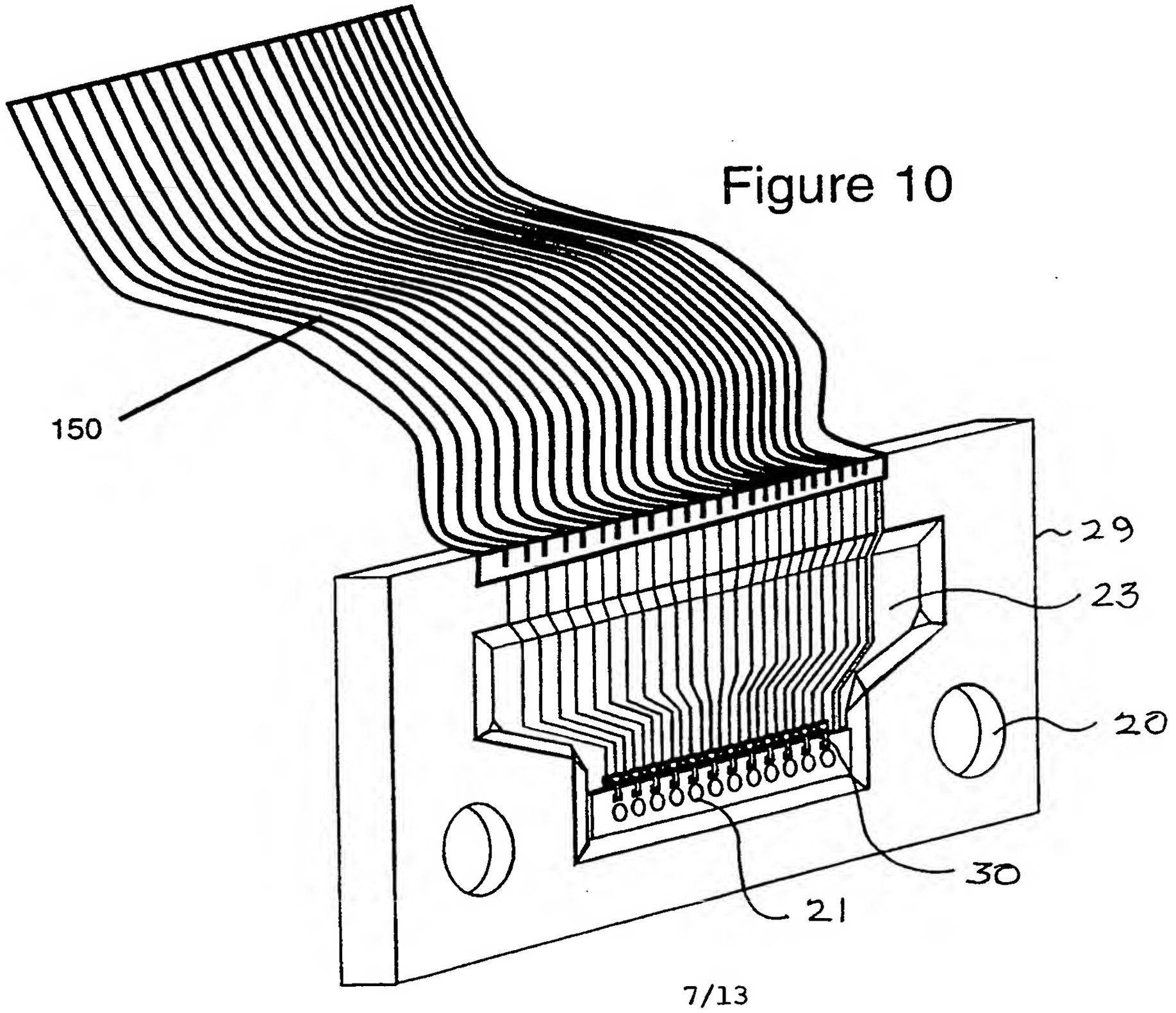


Figure 10



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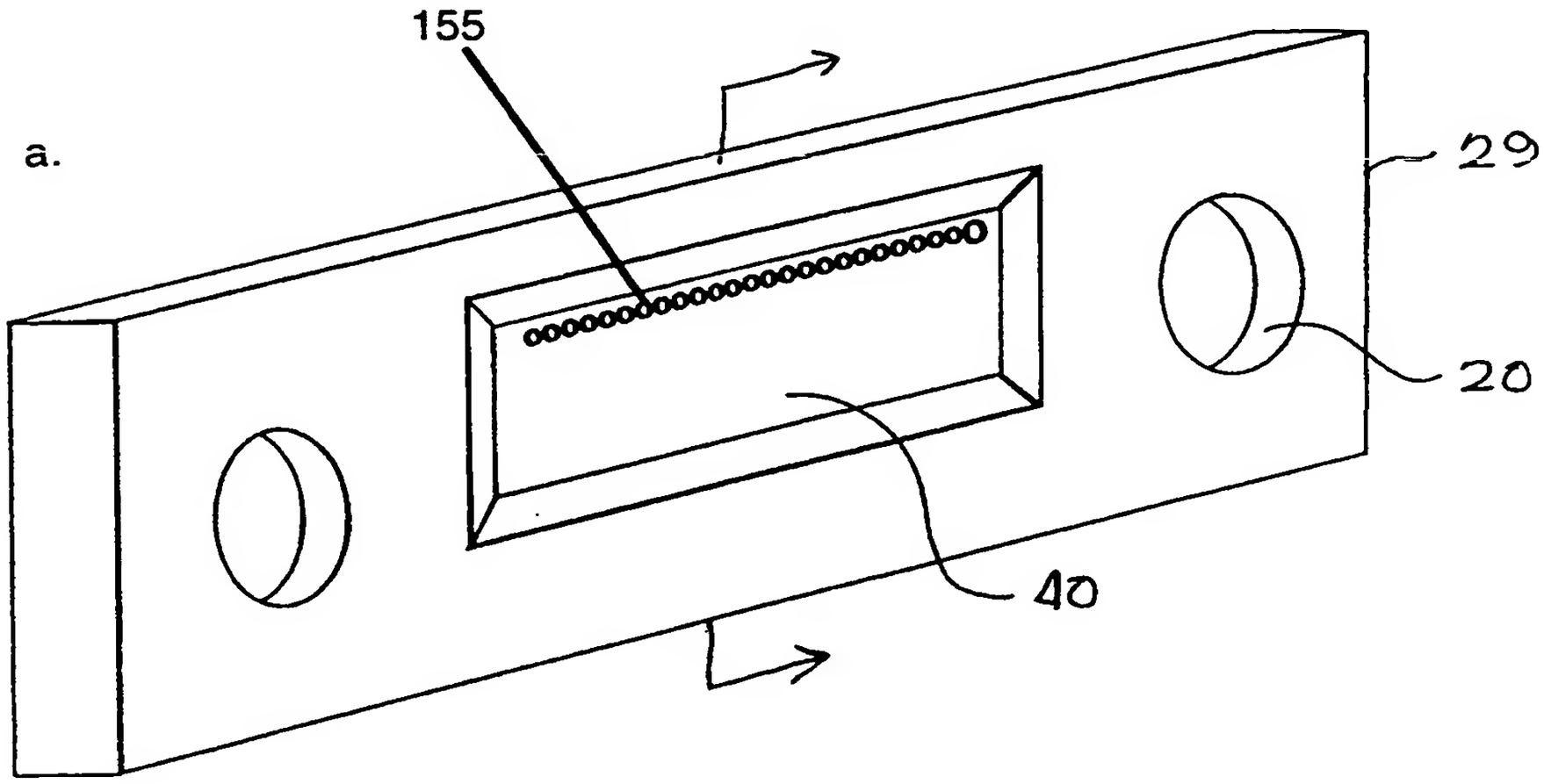

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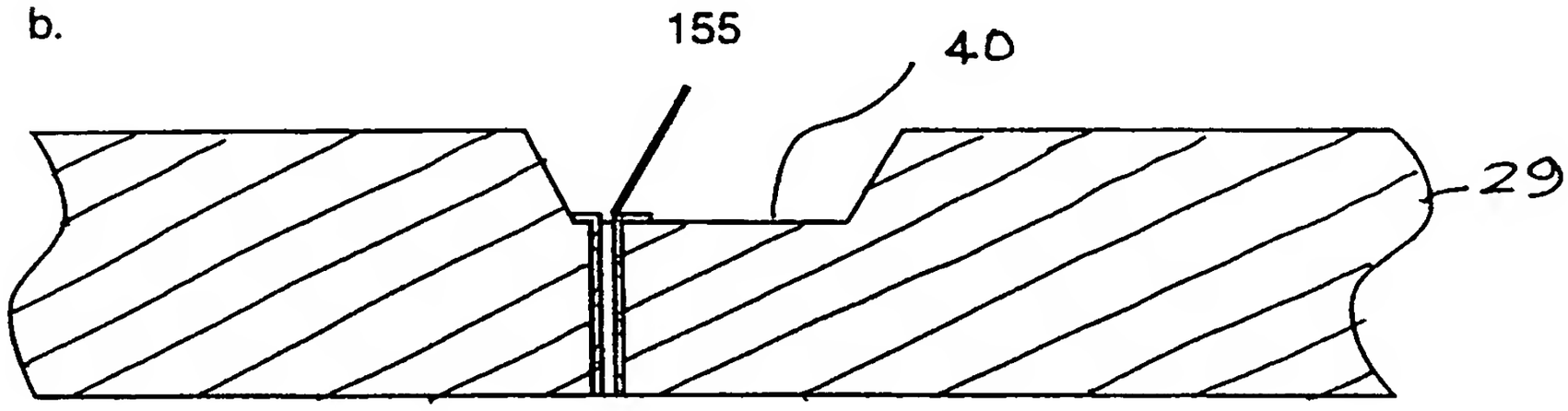

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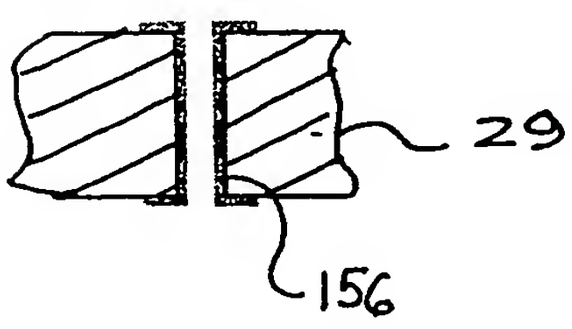

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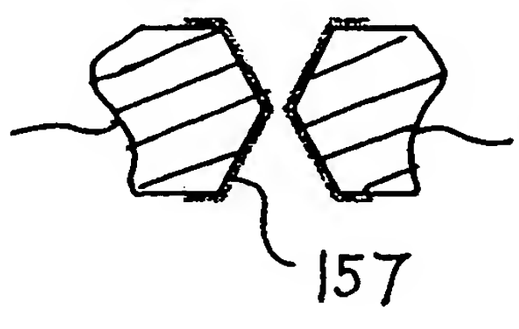

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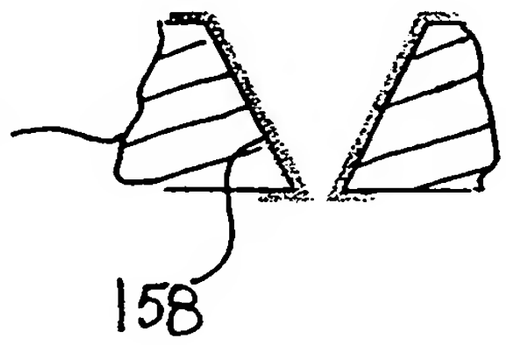

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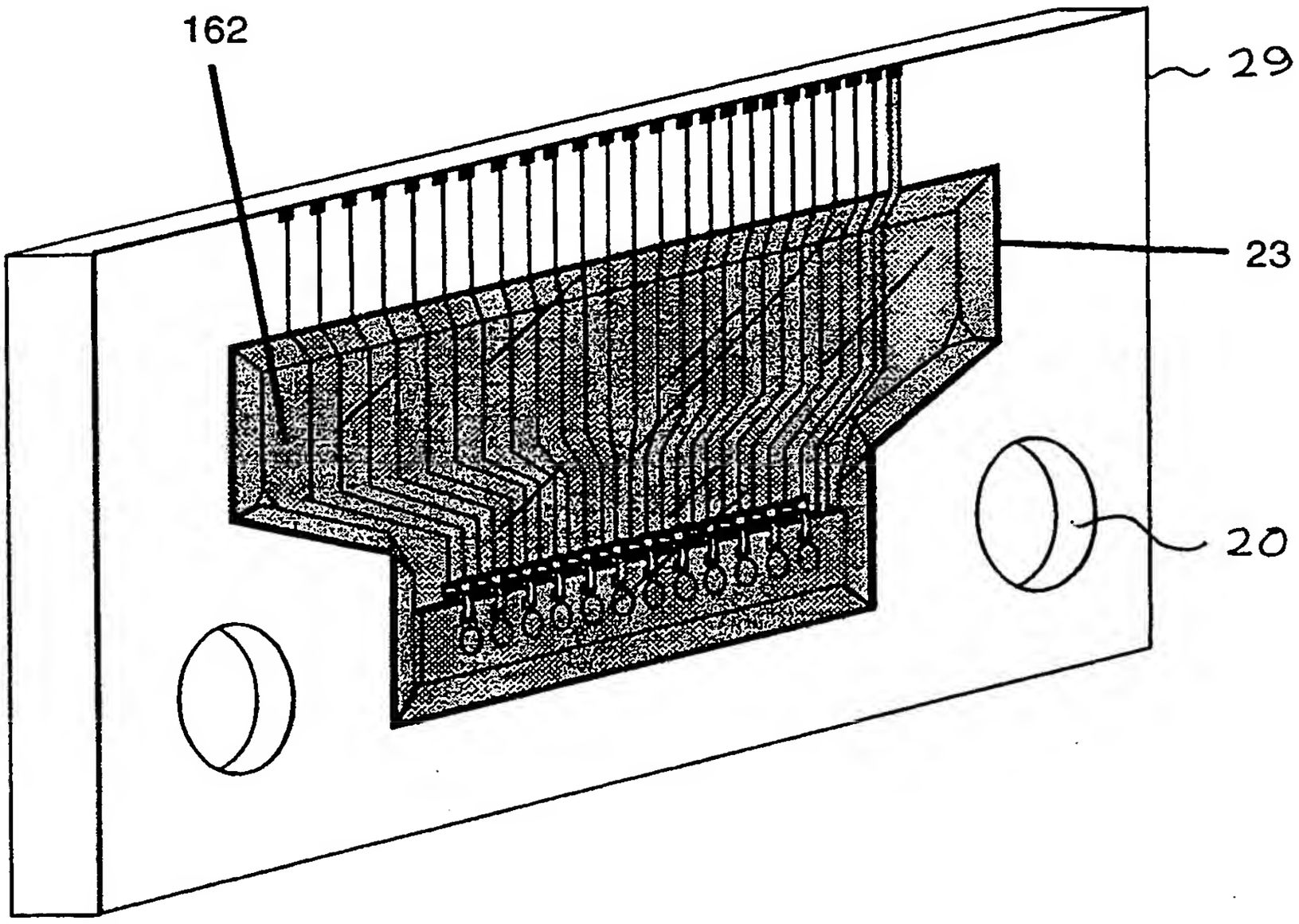

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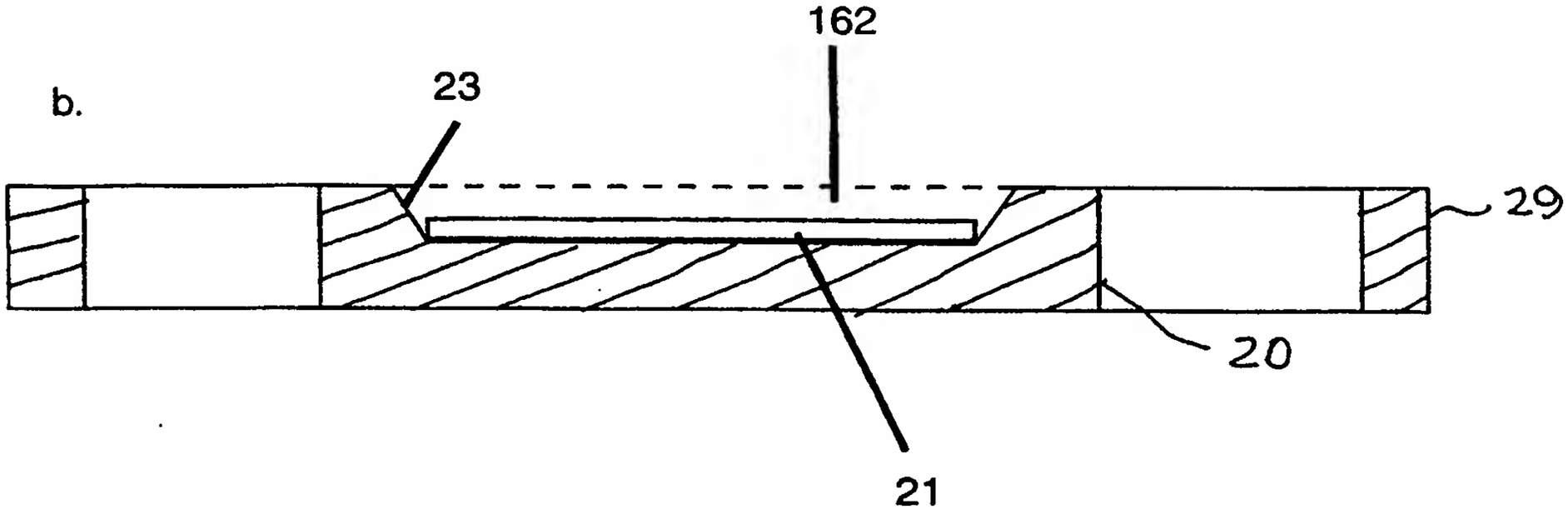
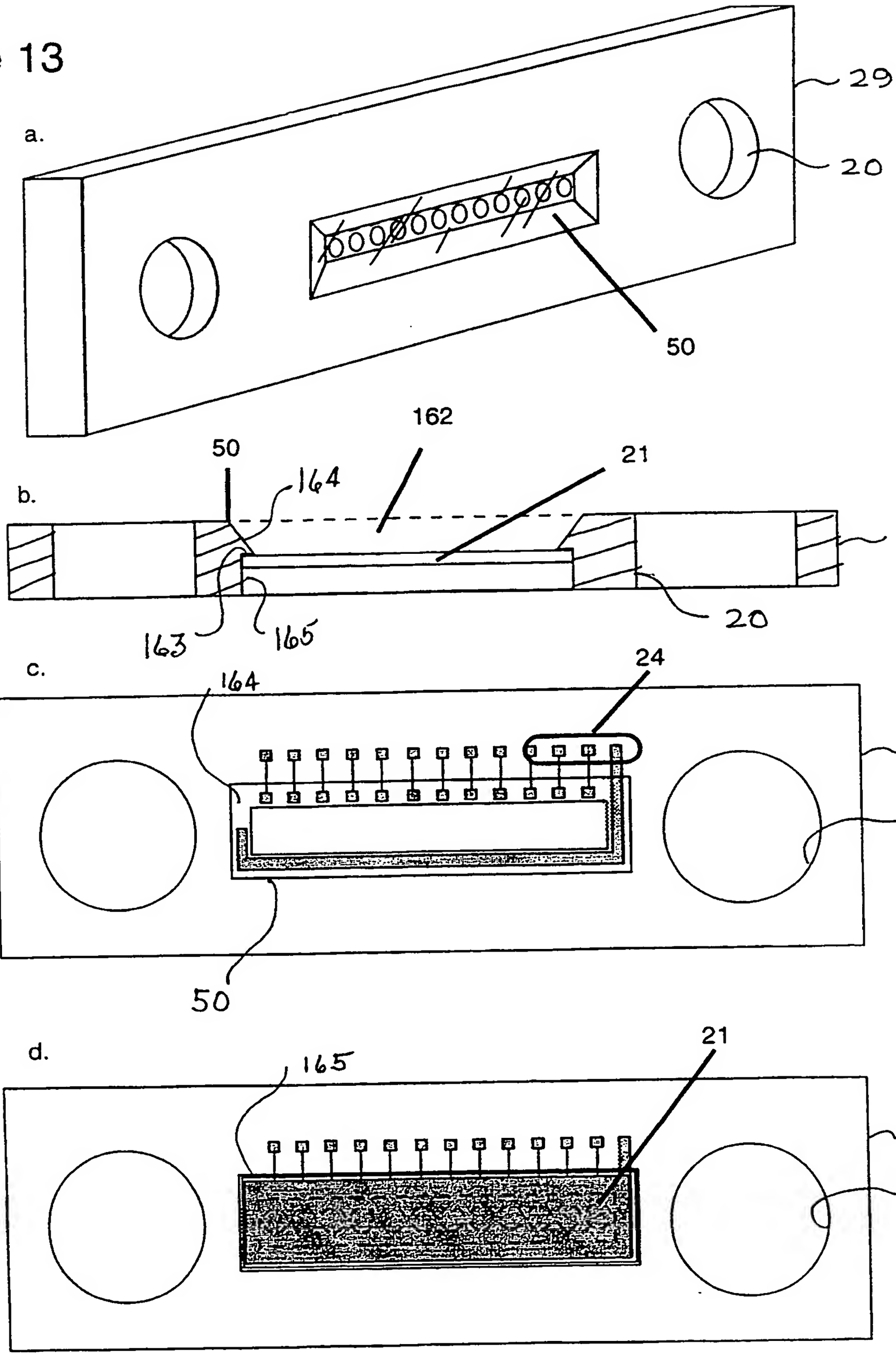


Figure 13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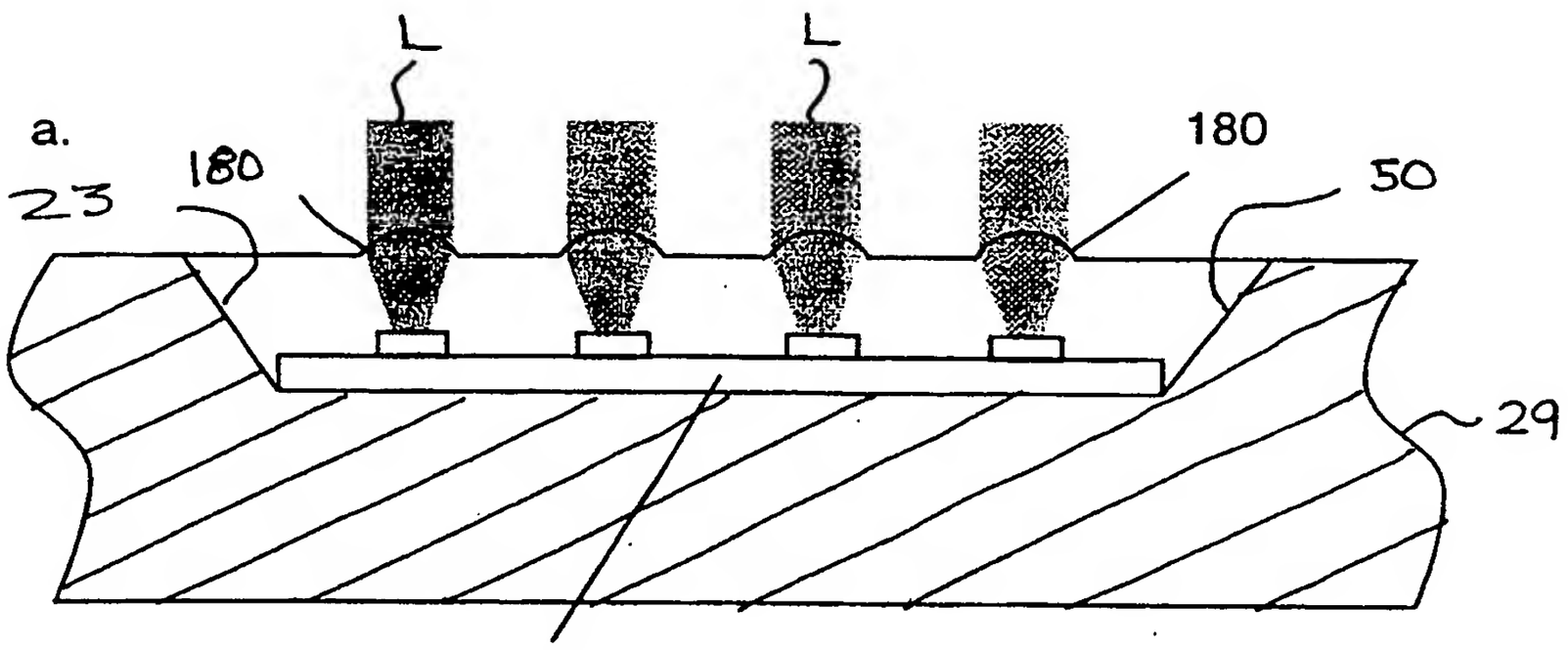

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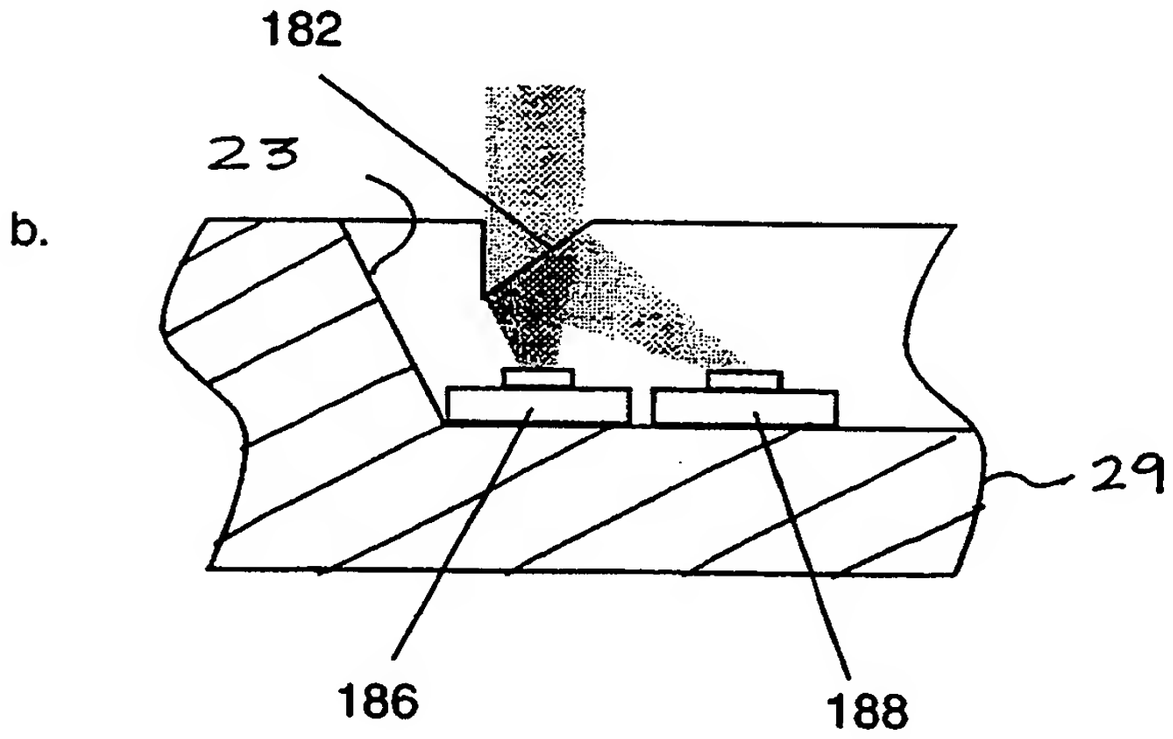

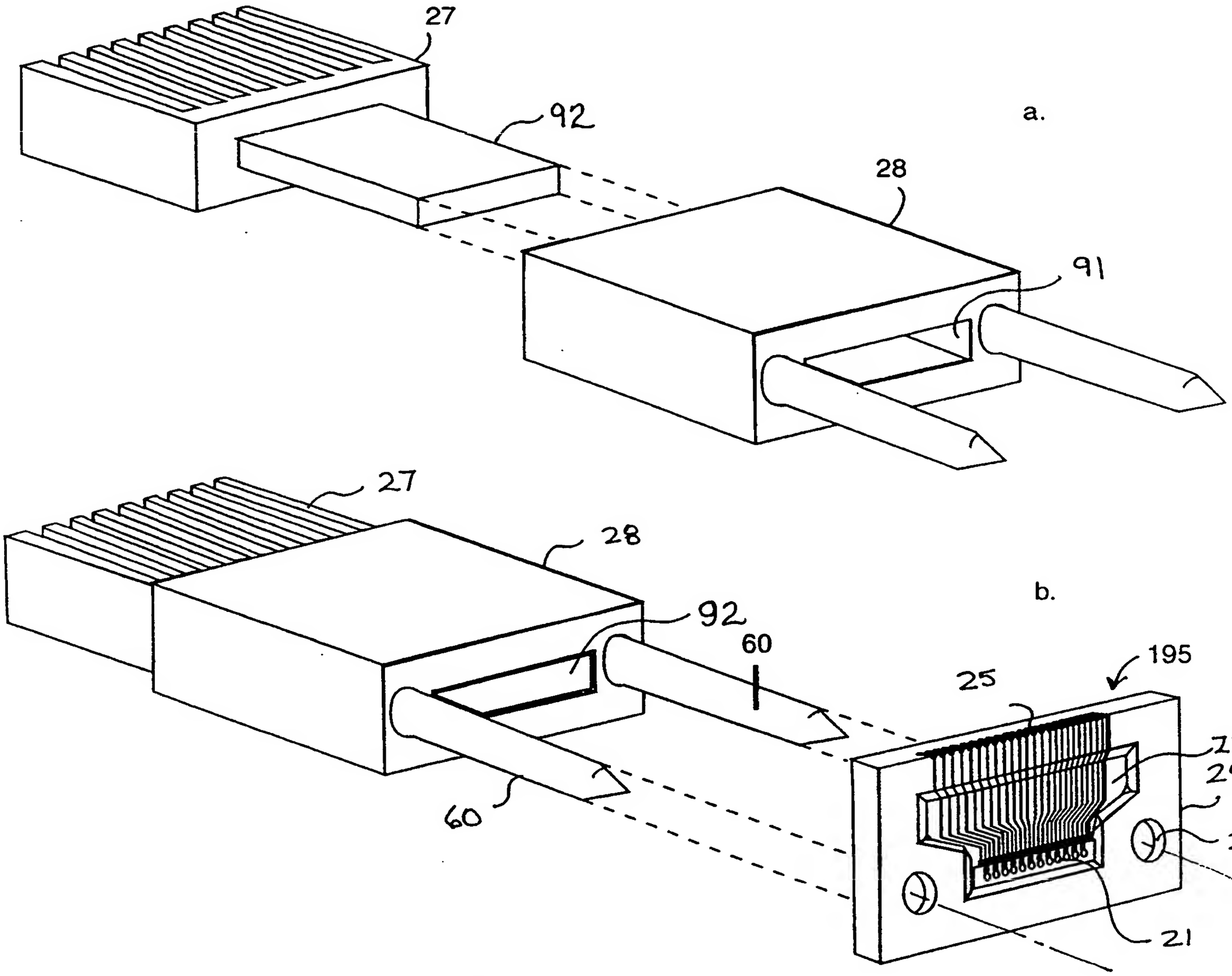
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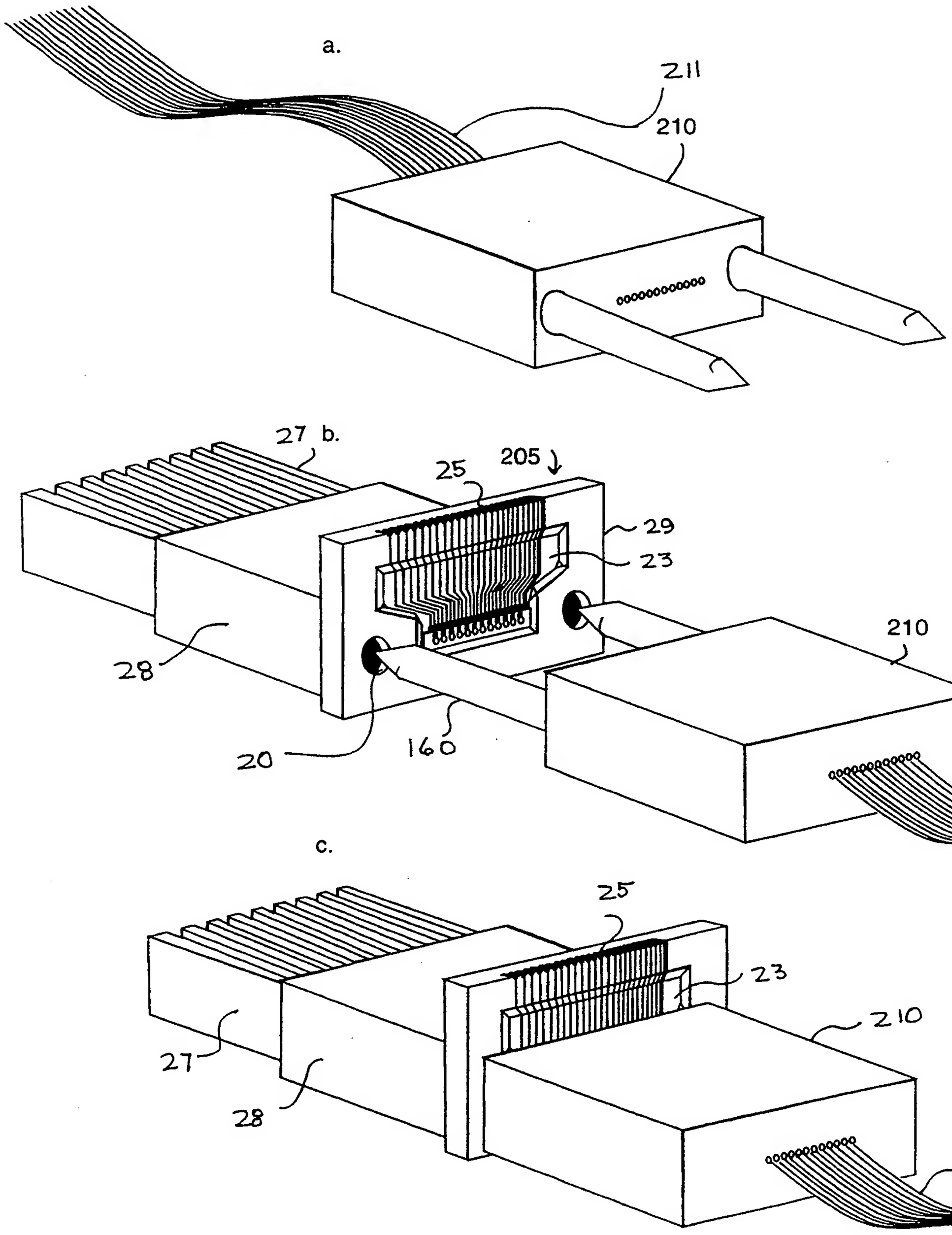
Figure 16



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/01673

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01J 5/02
US CL :250/239

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 250/239, 551; 385/52, 53, 54, 55, 65, 88, 89, 99

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international searoh (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,091,991 A (BRIGGS et al) 25 February 1992 (25/02/92), see entire document.	1,4,8,19,23,29,38,43-45,50-52,65
Y		2,3,5-7,9-18,20-22,24-28,30-37,39-42,46-49,53-64,66
A	US 5,281,301 A (BASAVANHALLY) 25 January 1994 (25/01/94), see entire document.	1-66

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
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